Fall 2012
Lec IS 117 M 12:00 – 1:50PM
Office Hours:
M: 2- 3:00 PM
W: 11- 12:00 noon

Instructor: Tom Brown, Jr.
Office: IS 101
Phone (408) 924-3211

Course Description

Semiconductor theory; p-n junction, bipolar transistors, JFET's and MOSFETs, optoelectronic devices. Operational amplifiers and 555 timers. Device applications: comparators, signal generators, active filters, instrumentation amplifiers, voltage regulators, and power supplies.

Student Learning Objectives

Upon successful completion of this course, students will be able to:

a) Describe the fundamentals of semiconductor diodes, transistors, op-amps, timers, and oscillators.

b) Build, identify, and analyze diode circuits, transistor circuits, op-amp circuits, active filters, and oscillators.

c) Design or modify fundamental electronic circuits to meet certain requirements.

Textbook

# Course Evaluation

## Examinations

<table>
<thead>
<tr>
<th>Examination #</th>
<th>Date</th>
<th>Weight</th>
<th>Total</th>
</tr>
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<tbody>
<tr>
<td>#1</td>
<td>Oct 08</td>
<td>10%</td>
<td>100 pts</td>
</tr>
<tr>
<td>#2</td>
<td>Nov 26</td>
<td>10%</td>
<td>100</td>
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## Quizzes

<table>
<thead>
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<th>Quiz #</th>
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<tbody>
<tr>
<td>#1</td>
<td>Sep 17</td>
<td>5%</td>
<td>50</td>
</tr>
<tr>
<td>#2</td>
<td>Oct 29</td>
<td>5%</td>
<td>50</td>
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## Homework

<table>
<thead>
<tr>
<th>Assignment Type</th>
<th>Weight</th>
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<tbody>
<tr>
<td>Homework</td>
<td>10%</td>
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## Lab

<table>
<thead>
<tr>
<th>Type</th>
<th>Weight</th>
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<tbody>
<tr>
<td>Lab</td>
<td>35%</td>
<td>350</td>
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</table>

## Final

- **Date**: Dec 18, Tu, Rm IS117
- **Time**: 9:45 – 12:00 noon
- **Weight**: 25%
- **Total**: 250 pts

**Total**: 100% 1000 pts

## Grading

The final grade will be determined according to the following scale:

- **A+**: 97 - 100%
- **A**: 93 - 96%
- **A-**: 90 - 92%
- **B+**: 87 - 89%
- **B**: 83 - 86%
- **B-**: 80 - 82%
- **C+**: 77 - 79%
- **C**: 73 - 76%
- **C-**: 70 - 72%
- **D+**: 66 - 69%
- **D**: 60 - 65%
- **F**: 00 - 59%

## I. Examinations & Quizzes

There will be two examinations and two quizzes given during the semester, unexcused absences will lead to a zero grade.

## II. Homework Assignments

Homework is due at the beginning of each Monday class session. Late homework will not be accepted.
**Academic Integrity Policy:**
Your own commitment to learning, as evidenced by your enrollment at San Jose State University, and the university's Academic Integrity Policy requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the Office of Student Conduct and Ethical Development. The policy on academic integrity can be found at http://sa.sjsu.edu/student_conduct.

**Americans with Disabilities Act Policies:**
If you need course adaptations or accommodations because of a disability, or if you need special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with DRC to establish a record of their disability.
<table>
<thead>
<tr>
<th>Week Of</th>
<th>Lecture Topics</th>
<th>Problems</th>
</tr>
</thead>
</table>
| 8/27     | Ch 2: Diodes And Applications  
2-1: Diode Operation  
2-2: Voltage-Current Characteristic (Diode)  
2-3: Diode Models | 2-3: 7,8         |
| 9/10     | 2-4: Half-Wave Rectifiers  
2-5: Full-Wave Rectifiers  
2-6: Power Supply Filters and Regulators | 2-4: 9,11,13  
2-5: 15,16,17,19  
2-6: 23,25,27,29 |
| 9/17     | Ch 3: Special-Purpose Diodes  
3-1: The Zener Diode  
3-2: Zener Diode Applications | 3-1: 1,2,3,5  
3-2: 6,7,8,9,10,11,12,13,14,15  
3-6: 30 |
| 9/24     | Ch 4: Bipolar Junction Transistors  
4-1: BJT Structure  
4-2: Basic BJT Operations  
4-3: BJT Characteristics And Parameters  
4-4: The BJT As An Amplifier | 4-3: 7,9,11,14,15,16,17,19,21  
4-4: 25,27 |
| 10/1     | 4-5: The BJT As A Switch  
5-1: The DC Operating Point  
5-2: Voltage Divider Bias  
5-3: Emitter, Base, Emitter-Feedback And Collector-Feedback Biasing | 4-5: 29,30  
5-1: 1,2,3,4,5,7,8,9  
5-2: 11,12,14,15,17  
5-3: 19,21,23,27  
5-4: 35 |
| 10/8     | Examination #1                                  |                  |
| 10/15    | 6-1: Amplifier Operations  
6-2: Transistor AC Models  
6-3: The Common-Emitter Amplifier  
6-4: The Common-Collector Amplifier | 6-3: 7,8,9,10,11,12,13,14,19  
6-4: 20,21,22,23,25 |
| 10/22    | 6-5: The Common-Base Amplifier  
6-6: Multistage Amplifiers | 6-5: 26,27,28  
6-6: 29,31,33,35 |
| 10/29    | 8-1: The JFET  
8-2: JFET Characteristics and Parameters  
8-3: JFET Biasing  
8-4: The Ohmic Region | 8-2: 5,8,7,9,10,11,13  
8-3: 16,17,18,19,21,23,24  
8-4: 28,29,30,31 |
| 11/5     | 9-1: The Common-Source Amplifier  
9-2: The Common-Drain Amplifier  
9-3: The Common-Gate Amplifier | 9-1: 1,3,8,9,11,13,14,15,16,17,18  
9-2: 24,25,26,27  
9-3: 28,29,30,31 |
| 11/19    | 10-3: Low-Frequency Amplifier Response  
10-4: High-Frequency Amplifier Response  
10-5: Total Amplifier Frequency Response | 10-3: 13,14,15  
10-4: 19  
10-5: 23,25 |
| 11/26    | Examination #2                                  |                  |
| 12/3     | 12-4: Op-Amps with Negative Feedback  
12-5: Effects of Negative Feedback on Op-Amp Impedances  
12-7: Open-Loop Response  
12-8: Closed-Loop Response | 12-4: 11,13,15,16,17  
12-5: 19 |
| 12/10    | 13-1: Comparators  
13-2: Summing Amplifiers  
13-3: Integrators and Differentiators  
Ch 16: Oscillators | 13-1: 1,2,5  
13-2: 9,11,13 |
| 12/18    | Final, Rm. IS117, Time: 9:45-12:00 noon         |                  |