San José State University
Department of Aviation & Technology
Tech 62, Analog Circuits, Section 2, Fall 2018

Course and Contact Information

Instructor: Dr. Mostafa Mortezaie
Office Location: EIS216
Telephone: (408) 306-1919
Email: Mostafa.mortezaie@sjsu.edu, and CANVAS
Office Hours: T/Th: 15:50 to 16:50
Class Days/Time: T/Th: 15:00-15:50
Classroom: IS216
Prerequisites: TECH 060 and MATH 071 or MATH 030

Course Format:
The course relies on lecture materials presented in class and students are strongly encouraged to attend.

Course Description
Semiconductor theory; p-n junction, bipolar transistors, JFETs and MOSFETs, optoelectronic devices. Operational amplifiers and 555 timers. Device applications: comparators, signal generators, active filters, instrumentation amplifiers, voltage regulators and power supplies. Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

1. Describe the fundamentals of semiconductor diodes, transistors, op-amps, timers, and oscillators.
2. Build, identify, and analyze diode circuits, transistor circuits, op-amp circuits, active filters, and oscillators.
3. Design or modify fundamental electronic circuits to meet certain requirements

Required Texts/Readings

Textbook

Other Readings
Instructor lecture notes and datasheets.
For LTspice Exercises, download from the Link:
Course Requirements and Assignments

Class Participation
Homework assignments can be found posted on Canvas (https://sjsu.instructure.com). Click on the Modules tab. You need to include the question and the answer using MS-Word document. The answers should be easy to follow.

Class Participation contributes to CLOs 2 and 3, learning the fundamental concepts of analog circuits, developing teamwork skills and discussing the course material.

Lab experiments
You will complete lab assignments individually using the SPICE software. In addition, you will hardware 4 lab experiments and will compare the measurements obtained using real instruments with the ones obtained using SPICE. The written reports will be submitted one week after the date of the assigned lab. Lab experiments contribute to CLOs 2, 4 and 5, reinforcing the course material and developing teamwork skills.

Tests
You will take weekly take-home quizzes, two midterms and the final exam. Tests will start and end at the scheduled time. These tests contribute to CLOs 1, 2 and 3 as well as reinforcing the learning of the fundamental concepts of analog circuits.

Final Examination or Evaluation
Final Exam will be as shown below:

| Monday, December 17 | 1445-1700 |

Grading Information
Weekly online Quizzes, midterms and final exam will be graded based on the followed process and accurate answers. Class Participation will be evaluated based on the followed process and percent of accurate responses provided. Lab experiments grade will be determined on the percent of lab assignments completed on or before the due date.

Determination of Grades
Grades will be determined based on your performance in Lab experiments, Class Participation, Weekly Quizzes, Midterms and Final Exam. The final grade for the course will be based on the following items and weights:

1. Lab experiments 30%
2. Class participation online 5%
3. Homework Assignments 10%
4. Weekly Quizzes 15%
5. Midterms (2x10%) 20% (Midterm 1: October 4th and Midterm 2: Nov 1st)
6. Final Exam 20% (Final Exam: December 17, 2018)

There will be no curving of grades. Final grades will be assigned as follows:
### Grading Scheme

<table>
<thead>
<tr>
<th>Name</th>
<th>Range:</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>100 % to 94.0%</td>
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<tr>
<td>A-</td>
<td>&lt; 94.0 % to 90.0%</td>
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<tr>
<td>B+</td>
<td>&lt; 90.0 % to 87.0%</td>
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<tr>
<td>B</td>
<td>&lt; 87.0 % to 84.0%</td>
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<tr>
<td>B-</td>
<td>&lt; 84.0 % to 80.0%</td>
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<td>C+</td>
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<td>C</td>
<td>&lt; 77.0 % to 74.0%</td>
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<td>C-</td>
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<td>D+</td>
<td>&lt; 70.0 % to 67.0%</td>
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<td>D</td>
<td>&lt; 67.0 % to 64.0%</td>
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<tr>
<td>D-</td>
<td>&lt; 64.0 % to 61.0%</td>
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<tr>
<td>F</td>
<td>&lt; 61.0 % to 0.0%</td>
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### University Policies

Per University Policy S16-9, Office of Graduate and Undergraduate Programs maintains university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs’ (GUP) Syllabus Information web page at:

[http://www.sjsu.edu/gup/syllabusinfo/](http://www.sjsu.edu/gup/syllabusinfo/)
## Course Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Topics, Readings, Assignments, Deadlines</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Aug 21, 23</td>
<td>Introduction/Orientation/Greensheet&lt;br&gt;Email Proof of completion of course prereq (Tech 60 or equivalent and MATH 71 or MATH 30) by 8/29&lt;br&gt;Read Ch1: Introduction to Electronics/Ch 2: Diodes&lt;br&gt;Watch video: <a href="http://www.youtube.com/watch?v=lA6V205VMyY">http://www.youtube.com/watch?v=lA6V205VMyY</a>&lt;br&gt;1-4: The PN junction&lt;br&gt;2-1: Diode Operation&lt;br&gt;2-3: Diode Models&lt;br&gt;LOAD LTSPICE: Set up for LAB&lt;br&gt;&lt;em&gt;Prepare in advance for the next session:&lt;/em&gt;&lt;br&gt;Watch video: <a href="http://www.youtube.com/watch?v=-td7YT-Pums&amp;feature=related">http://www.youtube.com/watch?v=-td7YT-Pums&amp;feature=related</a>&lt;br&gt;Read Chapter 4&lt;br&gt;Answer Problems Set 1</td>
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<tr>
<td>2</td>
<td>Aug 28, 30</td>
<td>Lecture: Chapter 4&lt;br&gt;4-1: BJT Structure&lt;br&gt;4-2: Basic BJT Operation&lt;br&gt;4-3: BJT Characteristics And Parameters&lt;br&gt;Email Proof of completion of course prereq (Tech 60 or equivalent and MATH 71 or MATH 30) by 8/30&lt;br&gt;4-4: The BJT As An Amplifier&lt;br&gt;4-5: The BJT As A Switch&lt;br&gt;Prepare Quiz Set1&lt;br&gt;• Submit Weekly Quiz 1 via Canvas when available&lt;br&gt;Attempt Assignment Set 1&lt;br&gt;Prepare in advance for the next session:&lt;br&gt;Watch video: <a href="https://www.youtube.com/watch?v=WLYc6oD2BYA">https://www.youtube.com/watch?v=WLYc6oD2BYA</a>&lt;br&gt;Read: Chapter 5&lt;br&gt;Finish Assignment Set 1</td>
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<td>3</td>
<td>Sep 4, 6</td>
<td>Lecture: Chapter 5&lt;br&gt;5-1: The DC Operating Point&lt;br&gt;5-2: Voltage Divider Bias&lt;br&gt;5-3: Emitter, Base, Emitter-Feedback And Collector-Feedback Biasing&lt;br&gt;&lt;strong&gt;Finish Problems Set 2&lt;br&gt;Submit Weekly Quiz 2 via Canvas. Click on the Assignments tab.&lt;br&gt;&lt;em&gt;Prepare in advance for the next session:&lt;/em&gt; Read Chapter 6&lt;br&gt;Watch video: <a href="https://www.youtube.com/watch?v=Pkjn18Ekjic">https://www.youtube.com/watch?v=Pkjn18Ekjic</a>&lt;br&gt;Read 6-3: The Common-Emitter Amplifier&lt;br&gt;Read 6-4: The Common-Collector Amplifier&lt;br&gt;Answer Problems Set 3</td>
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<tr>
<td>Week</td>
<td>Date</td>
<td>Topics, Readings, Assignments, Deadlines</td>
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| 4,5  | Sep 11, 13,18, 20 | Lecture: Chapter 6  
**Read** 6-1: Amplifier Operation  
**Watch** video: http://www.youtube.com/watch?v=-LPALAwcYkg  
**Read** 6-2: Transistor AC Models  
Finish Problems Set 3  
Submit Problems Set 2 via Canvas. Click on the **Assignments** tab.  
Submit Weekly Quiz 3 via Canvas. Click on the **Assignments** tab.  
**Read in advance for the next session:**  
Chapter 6  
**Answer Problems Set 4** |
| 6    | Sep 25, 27 | Lecture: Chapter 6  
6-5: The Common-Base Amplifier  
6-6: Multistage Amplifiers  
Finish Problems Set 4  
Submit Problems Set 3 via Canvas, Click on the **Assignments** tab.  
Submit Weekly Quiz 4 via Canvas.) Click on the **Assignments** tab.  
**Prepare in advance for the next session:**  
**Answer Problems Set 5**  
**Read in advance for the next session:**  
Chapter 8  
**Watch** video: http://www.youtube.com/watch?v=BzsXNhigVC0  
**Prepare for Midterm 1** |
| 7    | Oct 2, 4  | **Midterm 1, Oct 4**  
Lecture: Chapter 8  
8-1: The JFET  
8-2: JFET Characteristic and Parameters  
8-3: JFET Biasing  
8-4: The Ohmic Region  
Finish Problems Set 5  
Submit Problems Set 4 via Canvas. Click on the **Assignments** tab.  
Submit Weekly Quiz 5 via Canvas. Click on the **Assignments** tab. |
| 8    | Oct 9, 11 | **Review Q & A** |
| 9    | Oct 16, 18 | **Lecture:** Chapter 9  
**Read** 9-1: The Common-Source Amplifier  
**Read** 9-2: The Common-Drain Amplifier  
**Read** 9-3: The Common-Gate Amplifier  
**Answer Problems Set 6** |
<table>
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<tr>
<th>Week</th>
<th>Date</th>
<th>Topics, Readings, Assignments, Deadlines</th>
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</table>
| 10   | Oct 23, 25 | Discuss Chapter 10  
Finish Problems Set 7  
Submit Problems Set 6  
Submit Weekly Quiz 7  
*Prepare in advance for the next session:*  
Watch video: http://www.youtube.com/watch?v=TQB1VILBgJE  
Answer Problems Set 8 |
| 11   | Oct 30, Nov 1 | **Midterm 2, Nov 1**  
Lecture: Chapter 12  
12-4: Op-Amps with Negative Feedback  
12-5: Effects of Negative Feedback on Op-Amp Impedance  
12-7: Open-Loop Response  
12-8: Closed-Loop Response  
Finish Problems Set 8  
Submit Problems Set 7 via Canvas. Click on the Assignments tab.  
Submit Weekly Quiz 8 via Canvas. Click on the Assignments tab.  
*Prepare in advance for the next session:*  
Answer Problems Set 9  
Watch video: http://www.youtube.com/watch?v=nG8gA_kAp-Y |
| 12, 13 | Nov 6, 8, 13, 15 | Lecture: Chapters 13 & 16  
13-1: Comparators  
13-2: Summing Amplifiers  
13-3: Integrators and Differentiators  
16-2: Feedback Oscillator Principles and Oscillator types  
13-3: Integrators and Differentiators  
16-2: Feedback Oscillator Principles and Oscillator types  
Finish Problems Set 9  
Submit Problems Set 8 via Canvas. Click on the Assignments tab.  
Submit Weekly Quiz 9 via Canvas. Click on the Assignments tab.  
*Prepare in advance for the next session:*  
Watch video: http://www.youtube.com/watch?v=yj4uVVV5Nsg  
Answer Problems Set 10 |
| 14   | Nov 20, 22  
Thanks Giving Nov 22 | Lecture: Chapter 2  
Read 2-4: Half-Wave Rectifiers  
Read 2-5: Full-Wave Rectifiers  
Review Q & A  
Finish Problems Set 10  
Submit Problems Set 9 via Canvas. Click on the Assignments tab.  
Submit Weekly Quiz 10 via Canvas. Click on the Assignments tab. *Due by 11:00 pm on 11/29! Individual submission* |
<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Topics, Readings, Assignments, Deadlines</th>
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<tbody>
<tr>
<td>15</td>
<td>Nov 27, 29</td>
<td><strong>Prepare in advance for the next session:</strong></td>
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<tr>
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<td><strong>Lecture:</strong> Chapter 2</td>
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<td>2-6: Power Supply Filters and Regulators</td>
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<td><strong>Read</strong> Ch3: Special-Purpose Diodes</td>
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<td><strong>Watch</strong> video: <a href="http://www.youtube.com/watch?v=jG2YaTWxyc">http://www.youtube.com/watch?v=jG2YaTWxyc</a></td>
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<tr>
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<td><strong>Read</strong> 3-1: The Zener Diode</td>
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<td><strong>Read</strong> 3-2: Zener Diode Application</td>
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<td><strong>Answer Problems Set 11</strong></td>
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<td>16</td>
<td>Dec 4, 6</td>
<td>Review All material</td>
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<td><strong>Submit Problems Set 10 via Canvas. Click on the Assignments tab.</strong></td>
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<td><strong>Submit Problems Set 11 via Canvas. Click on the Assignments tab.</strong></td>
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<td><strong>Prepare for FINAL</strong></td>
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<td>Final Exam</td>
<td>Monday, Dec 17, 2018</td>
<td><strong>Venue: IS216</strong></td>
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<td>Monday, December 17 1445-1700</td>
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**SAN JOSE STATE UNIVERSITY**  
**Department of Aviation & Technology**  
Tech 62 Labs @ IS117  
Fall 2018  
Section  TBD  

**Office Hour:** TBD  
**TAs:** juidarshankumar.modi@sjsu.edu

<table>
<thead>
<tr>
<th>Week (dates subject to revision)</th>
<th>Lab Experiments</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>Hands On, Lab Safety and Rules by TAs. SPICE Introduction.</td>
</tr>
<tr>
<td>1&amp;2</td>
<td>SPICE Bipolar Transistor characteristics. Refer Experiment #11</td>
</tr>
<tr>
<td>1&amp;2</td>
<td>SPICE Collector-feedback biased BJT. Refer Experiment #16</td>
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</tbody>
</table>
| 2&3                             | #1 Hardwired lab Experiment  
Collector-feedback biased BJT (2N3904 or equivalent)  
BONUS: Bipolar Transistor characteristics |
| 3&4                             | SPICE Voltage Divider Biased BJT. Refer Experiment #13 |
| 4&5                             | #2 Hardwired Lab Experiment  
Voltage Divider Biased BJT |
| 6                               | SPICE Small-signal common-emitter amplifier. Refer Experiment #17 |
| 6&7                             | #3 Hardwired Lab Experiment  
Small-signal common-emitter amplifier |
| 8                               | SPICE JFET Small-signal common-source amplifier. Refer Experiment #27 |
| 8&9                             | SPICE OPAMP Inverting voltage amplifier. Refer Experiment #32  
SPICE OPAMP Non Inverting voltage amplifier. Refer Experiment #31 |
| 10                              | catch up |
| 11                              | #4 Hardwired Lab Experiment  
Inverting Voltage Amplifier |
| 14                              | Thanksgiving Holidays – Campus Closed (Thursday through Friday) |
| 15                              | SPICE Op-amp Integrator and Differentiator. Refer Experiment #35. |
| 16                              | Catch up  
BONUS: Hardwire Op-amp Integrator or Differentiator |

**Notes:**  
1. Each student will perform all lab experiments using SPICE: Simulation Program with Integrated Circuit Emphasis (LTspice/Multisim software).  
2. Each student will submit an online lab report a week after the lab is completed.  
3. Students working in groups of 2-3 members will hardwire four lab experiments. The measurements obtained in these hardwired lab experiments will be compared with the ones obtained using SPICE.  
4. While one batch of students work at the Computer Area other half will work on the instrument test benches area. Simulation and Hardwiring may be repeated in any order.  
5. Each group will submit a report online of each hardwired lab within week after the lab is completed.  
6. Experiment is complete when Report is complete and accepted. If you have finished the Lab data collection you may spend the rest of the time in Lab to complete the report and submit online.