San José State University  
Department of Aviation &Technology  
Tech-62, Analog Circuits, Section 1, Spring 2018

Course and Contact Information

Instructor: Dr. Mostafa Mortezaie
Office Location: IS216
Telephone: (408) 306-1919
Email: mostafamortezaie@yahoo.com, and CANVAS (preferred)

Office Hours: Tuesday: 14:30-15:00 & Thursday: 15:50 to 16:20 (IS126)
Class Days/Time: Tu/Th: 15:00-15:50
Classroom: IS126

Prerequisites: TECH-60 and MATH-071 or MATH-030

Course Format: The course relies on lecture materials presented in class and students are strongly encouraged to attend.

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas Learning Management System course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through MySJSU at http://my.sjsu.edu (or other communication system as indicated by the instructor) to learn of any updates.

Course Description

Semiconductor theory; p-n junction, bipolar transistors, JFETs and MOSFETs, optoelectronic devices. Operational amplifiers and 555 timers. Device applications: comparators, signal generators, active filters, instrumentation amplifiers, voltage regulators and power supplies. Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

1. Describe the fundamentals of semiconductor diodes, transistors, op-amps, timers, and oscillators.
2. Build, identify, and analyze diode circuits, transistor circuits, op-amp circuits, active filters, and oscillators.
3. Design or modify fundamental electronic circuits to meet certain requirements

Required Texts/Readings

Textbook
Other Readings
Instructor lecture notes and datasheets.
For LTspice Exercises, download from the Link:

Course Requirements and Assignments

Class Participation
Students working in groups of 2-3 will solve Problems Sets (assigned problems from each chapter) posted on Canvas (https://sjsu.instructure.com). Click on the Modules tab. You need to include the question and the answer. The answers should be easy to follow. The whole class will check/discuss if the answers are correct before submitting them. This group discussion will reinforce and/or enhance your analog circuits' knowledge.
Class Participation contributes to CLOs 2 and 3, learning the fundamental concepts of analog circuits, developing teamwork skills and discussing the course material. Class Participation is based on in class assignment or instructor observation of students’ participation and presence in the class. Classes missed without approved reason and not made up will deduct from this score.

Lab experiments
You will complete lab assignments individually using the SPICE software. In addition, you will hardwire 4 lab experiments and will compare the measurements obtained using laboratory measuring instruments with the simulation results obtained using SPICE. The written reports will be submitted one week after the date of the assigned lab. Lab experiments contribute to CLOs 2, 4 and 5, reinforcing the course material and developing teamwork skills.

Tests
You will be assigned quizzes on a regular intervals as indicated in the syllabus, two midterms and a final exam. Tests will start and end at the scheduled time. These tests contribute to CLOs 1, 2 and 3 as well as reinforcing the learning of the fundamental concepts of analog circuits.

Final Examination
Final Exam will be administered in class on Thursday, May 17, 2018, 2:45 PM to 5:00 PM.

Grading Information
Weekly online Quizzes, midterms, and final exam will be graded based on work shown and accurate answers. Class Participation is based on in-class assignments or instructor observation of students’ participation as well as class presence. Lab experiments grade will be determined by the percent of lab assignments completed on or before the due date.

Determination of Grades
Grades will be determined based on your performance in Lab experiments, Class Participation, Weekly Quizzes, Midterms, homework, and Final Exam. The final grade for the course will be based on the following items and weights:

1. Lab experiments 30%
2. Class participation online 5%
3. Homework Assignments 10%
4. Weekly Quizzes 15%
5. Midterms (2x10%) 20% (Midterm 1: March 6th , and Midterm 2 : April 5th)
6. Final Exam 20% (Final Exam: May 17th)
There will be no curve for grading. Final grades will be assigned as follows:

\[
\begin{align*}
A & : >94 \\
A- & : 90-93 \\
B+ & : 85-89 \\
B & : 80-84 \\
B- & : 76-79 \\
C+ & : 72-75 \\
C & : 69-71 \\
C- & : 65-68 \\
D+ & : 62-64 \\
D & : 59-61 \\
D- & : 56-58 \\
F & : <55
\end{align*}
\]

Classroom Protocol

1. You are expected to attend all meetings for the course as you are responsible for material covered in the syllabus. Active participation is essential to ensure maximum benefit for all students. Attendance is fundamental to course objectives; for example, you may be required to interact with others in the class.

2. Download (DO NOT print) read and bring softcopies of the assigned Chapter handout posted on Canvas (https://sjsu.instructure.com). Click on the Modules tab.

3. You will study the assigned chapter/material before coming to lecture by watching the assigned videos, reading the textbook and reviewing the PowerPoint presentation posted on Canvas (https://sjsu.instructure.com). Click on the Modules tab.

4. After reviewing the chapter materials you will answer the Problem Sets (assigned problems at the end of the chapter) posted on Canvas (https://sjsu.instructure.com). Click on the Modules tab.

5. Instructor will explain key points and answer questions from students. Instructor may add related material to enrich the course content.

6. Instructor will become more of a facilitator of the learning process. This means that the instructor will provide as much individual or group assistance as needed.

7. Students should work and learn in teams. This is very important to be successful in the real world.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs’ Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"
## Tech 62 Analog Circuits, Fall 2017 Course Schedule

The schedule is subject to change with one week notice on CANVAS and email.

### Course Schedule

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<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Topics, Readings, Assignments, Deadlines</th>
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<tbody>
<tr>
<td>1</td>
<td>JAN 25</td>
<td>Introduction/Orientation/Greensheet&lt;br&gt;<strong>Proof of completion of course prerequisite</strong> (Tech 60 or equivalent and MATH 71 or MATH 30)&lt;br&gt;<strong>Read</strong> Ch1: Introduction to Electronics</td>
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<tr>
<td>2</td>
<td>JAN 30 &amp; FEB 1</td>
<td>Chapter 2: Diodes&lt;br&gt;<strong>Watch</strong> video: <a href="http://www.youtube.com/watch?v=lA6V205VMYy">http://www.youtube.com/watch?v=lA6V205VMYy</a>&lt;br&gt;<strong>Read</strong> 1-4: The PN junction&lt;br&gt;<strong>Read</strong> 2-1: Diode Operation&lt;br&gt;<strong>Read</strong> 2-3: Diode Models&lt;br&gt;LOAD LTSPICE: Set up for LAB</td>
</tr>
<tr>
<td>3</td>
<td>FEB 6 &amp; FEB 8</td>
<td>Chapter 2 Continue&lt;br&gt;<strong>Watch</strong> video: <a href="http://www.youtube.com/watch?v=yjuVVV5Nsg">http://www.youtube.com/watch?v=yjuVVV5Nsg</a>&lt;br&gt;<strong>Read</strong> 2-4: Half-Wave Rectifiers&lt;br&gt;<strong>Read</strong> 2-5: Full-Wave Rectifiers&lt;br&gt;<strong>Problems Set 1</strong>&lt;br&gt;<strong>Quiz 1</strong></td>
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<tr>
<td>4</td>
<td>FEB 13 &amp; FEB 15</td>
<td>Download (DO NOT print) read and bring softcopies of Chapter 4&lt;br&gt;<strong>Modules</strong> tab.&lt;br&gt;<strong>Watch</strong> video: <a href="http://www.youtube.com/watch?v=td7YT-Pums&amp;feature=related">http://www.youtube.com/watch?v=td7YT-Pums&amp;feature=related</a>&lt;br&gt;<strong>Read</strong> Chapter 4:&lt;br&gt;4-1: BJT Structure&lt;br&gt;4-2: Basic BJT Operation&lt;br&gt;4-3: BJT Characteristics And Parameters&lt;br&gt;<strong>Problems Set 2</strong>&lt;br&gt;<strong>Quiz 2</strong></td>
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<tr>
<td>5</td>
<td>FEB 20 &amp; FEB 22</td>
<td>Chapter 4 Continue&lt;br&gt;4-4: The BJT As An Amplifier&lt;br&gt;4-5: The BJT As A Switch&lt;br&gt;<strong>Problems Set 3</strong>&lt;br&gt;<strong>Quiz 3</strong></td>
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<tr>
<td>6</td>
<td>FEB 27 &amp; MAR 1</td>
<td>Chapter 4-5&lt;br&gt;<strong>Watch</strong> video: <a href="https://www.youtube.com/watch?v=WLYc6oD2BYA">https://www.youtube.com/watch?v=WLYc6oD2BYA</a>&lt;br&gt;<strong>Read:</strong>&lt;br&gt;5-1: The DC Operating Point&lt;br&gt;5-2: Voltage Divider Bias&lt;br&gt;5-3: Emitter, Base, Emitter-Feedback And Collector-Feedback Biasing&lt;br&gt;<strong>Problems Set 4</strong>&lt;br&gt;<strong>Quiz 4</strong></td>
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| 7    | MAR 6 & MAR 8 | Review Chapter 5
Review Chapter 5
**Download (DO NOT print) read and bring softcopies of** Chapter 6 handout 2017 from Canvas. **Modules** tab.
**Read** 6-1: Amplifier Operation
**Watch** video: [LPALAwcYkg](http://www.youtube.com/watch?v=LPALAwcYkg)
**Read** 6-2: Transistor AC Models
**Watch** video: [Pkjn18Ekjic](https://www.youtube.com/watch?v=Pkjn18Ekjic)
**Read** 6-3: The Common-Emitter Amplifier
**Read** 6-4: The Common-Collector Amplifier
**Problems Set 5**
**Quiz 5**
**MIDTERM 1 (March 6th)** |
| 8    | MAR 13 & MAR 15 | Discuss Chapter 6
**Read** and bring Chapter 6 handout 2017 from Canvas. **Modules** tab.
**Read in advance for the next session:**
6-5: The Common-Base Amplifier
6-6: Multistage Amplifiers
**Problems Set 6**
**Quiz 6** |
| 9    | MAR 20 & MAR 22 | Discuss Chapter 6
**Prepare in advance for the next session:**
**Read** 8-1: The JFET
**Watch** video: [BzsXNhigVC0](http://www.youtube.com/watch?v=BzsXNhigVC0)
**Read** 8-2: JFET Characteristic and Parameters
**Read** 8-3: JFET Biasing
**Read** 8-4: The Ohmic Region
**Problems Set 7**
**Quiz 7** |
| 10   | MAR 27 & MAR 29 | **Spring Break** |
| 11   | APR 3 & APR 5  | Chapter 9
**Read** 9-1: The Common-Source Amplifier
**Read** 9-2: The Common-Drain Amplifier
**Read** 9-3: The Common-Gate Amplifier
**Problems Set 8**
**Quiz 8**
**Midterm 2 (April 5th)** |
| 12   | APR 10 & APR 12 | **Prepare in advance for the next session:**
**Download (DO NOT print) read and bring softcopies of** Chapter 3
**Read** 2-6: Power Supply Filters and Regulators
**Read** Ch3: Special-Purpose Diodes
**Watch** video: [jG2YAtTwxc](http://www.youtube.com/watch?v=jG2YAtTwxc)
**Read** 3-1: The Zener Diode
**Read** 3-2: Zener Diode Application |
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</thead>
</table>
| 13   | APR 17 & APR 19 | Watch video: http://www.youtube.com/watch?v=TQB1VILBgJE  
Read 12-4: Op-Amps with Negative Feedback  
Read 12-5: Effects of Negative Feedback on Op-Amp Impedance  
Read 12-7: Open-Loop Response  
Read 12-8: Closed-Loop Response  
Problems Set 9  
Quiz 9 |
| 14   | APR 24 & APR 26 | Discuss Chapter 12  
Prepare in advance for the next session:  
Watch video: http://www.youtube.com/watch?v=nG8gA_kAp-Y  
Read 13-1: Comparators  
Read 13-2: Summing Amplifiers  
Read 13-3: Integrators and Differentiators  
Problems Set 10  
Quiz 10 |
| 15   | MAY 1 & MAY 3  | Chapter 16  
Read 16-2: Feedback Oscillator Principles and Oscillator types.  
Read 16-3 to 16-5  
Read 16-6: 555 Timer. |
| 16   | MAY 8 & MAY 10 | Review All material  
Prepare for FINAL |
| **Final Exam** | MAY 17 | Location: IS216  
Time: 12:15-14:30 |
Your Weekly Assignment (dates subject to revision) | Lab Experiments
---|---
1 | Hands On, Lab Safety and Rules by TAs. SPICE Introduction.
1&2 | SPICE Bipolar Transistor characteristics. Refer Experiment #11
1&2 | SPICE Collector-feedback biased BJT. Refer Experiment #16
2&3 | #1 Hardwired lab Experiment
Collector-feedback biased BJT (2N3904 or equivalent)
BONUS: Bipolar Transistor characteristics
3&4 | SPICE Voltage Divider Biased BJT. Refer Experiment #13
4&5 | #2 Hardwired Lab Experiment
Voltage Divider Biased BJT
6 | SPICE Small-signal common-emitter amplifier. Refer Experiment #17
6&7 | #3 Hardwired Lab Experiment
Small-signal common-emitter amplifier
8 | SPICE JFET Small-signal common-source amplifier. Refer Experiment #27
8&9 | SPICE OPAMP Inverting voltage amplifier. Refer Experiment #32
| SPICE OPAMP Non Inverting voltage amplifier. Refer Experiment #31
10 | #4 Hardwired Lab Experiment
Inverting Voltage Amplifier
12 | |
13/12 | SPICE Op-amp Integrator and Differentiator. Refer Experiment #35.
14/13 | Catch up
BONUS: Hardwire Op-amp Integrator or Differentiator

Notes:
1. Each student will perform all lab experiments using SPICE: Simulation Program with Integrated Circuit Emphasis (LTspice/Multisim software).
2. Each student will submit an online lab report a week after the lab is completed.
3. Students working in groups of 2-3 members will hardwire four lab experiments. The measurements obtained in these hardwired lab experiments will be compared with the simulation results using SPICE.
4. While one group of students work at the Computer Area other group will work on the instrument test bench area. Simulation and Hardwiring may be repeated in any order.
5. Each team will submit a report online of each hardwired lab within a week after the lab is completed.
6. Experiment is complete when the report is complete and accepted. If you have finished the Lab data collection you may spend the rest of the time in Lab to complete the report and submit online.