San José State University
Computer Science Department
CS 147, Section 03
Introduction to Computer Architecture
Fall, 2015

Course and Contact Information

Instructor: Kaushik Patra
Office Location: DH 282
Telephone: (408) 924-5161
Email: kaushik.patra@sjsu.edu
Office Hours: Mon/Wed 4:30 pm – 5:45 pm
Class Days/Time: MW 7:30 pm – 8:45 pm
Classroom: MH 223
Prerequisites: CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)

Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Topics:

Hardware Description Languages, Data Representation in Computer Hardware, Computer Arithmetic, Memory Organization, Control Unit Operation and Implementation, Instruction Formats, Pipelining and Vector Processing, Multiprocessing, and RISC Architecture and Principles.

Course Objectives:

• Review the basic Boolean number representation schemes, digital logic gates, and basic combinatorial and sequential circuit structures.

• Introduction to the basic roles and responsibilities for each of the major hardware components of a computer.
• Review the need to use a memory hierarchy, perform memory management, and to explain to them the various memory management techniques and their tradeoffs.

• Review implementation of the fundamental mathematical operations such as addition, subtraction, multiplication, and division and optimization with Boolean operands.

• Review tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).

• Review non-classical architectures such as parallel processors and pipelined machines which are used to accelerate hardware performance without impacting legacy sequential software programming languages or techniques.

• Introduction to computer-aided design tools and hardware description languages useful to computer architects in performing functional verification and performance measurements of digital systems.

• Review operation of hardware and software working synergistically together.

Learning Outcomes and Course Goals

Course Goal:

To examine alternative organizations and architectures associated with the implementation of basic computer hardware functions such as the memory hierarchy and its management, central processing unit (CPU) and arithmetic logic unit (ALU), instruction sets, and RISC.

Course Learning Outcomes (CLO):

Upon successful completion of this course, students should be able to:

• Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.

• Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.

• Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.

• Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.

• Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.

• Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.

• Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
• Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.

• Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.

• Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.

• Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware designs.

**BS in Computer Science Program Outcomes Supported:**

These are the BSCS Program Outcomes supported by this course:

a) An ability to apply knowledge of computing and mathematics to solve problems.

b) An ability to analyze a problem, to identify and define the computing requirements appropriate to its solution

c) An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs

d) An ability to use current techniques, skills, and tools necessary for computing practice

e) An ability to apply mathematical foundations, algorithmic principles, and computer science theory in the modeling and design of computer-based systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

**Required Texts/Readings** – can be rented or bought used/new from SJSU bookstore

**Textbook**

COMPUTER ORGANIZATION and DESIGN | Edition: 5
Author: DAVID A. PATTERSON
ISBN:9780124077263
Publication Date:10/10/2013
Publisher:ELSEVIER

**Other Readings**

COMPUTER ARCHITECTURE | Edition: 5TH 12
Author: HENNESSY
ISBN: 9780123838728
Publication Date: 09/29/2011
Publisher: ELSEVIER

LOGIC & COMPUTER DESIGN FUNDAMENTALS
Author: MANO & KIME
ISBN: 9780131989269
Publication Date: 06/15/2007
Publisher: PEARSON
Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in University Policy S12-3 at http://www.sjsu.edu/senate/docs/S12-3.pdf.

- Each student is expected to be present, punctual, and prepared at every scheduled class and lab session. It is assumed that the students already have basic knowledge of digital Boolean logic and fundamentals of assembly language machine programming.
- You will be required to bring a wireless laptop to all classes.
- Each class session will have lecture and hands on components. The lecture will be delivered in class room live, and hands on will be delivered as recorded video. One part of the class will be used to discuss hands on issues—therefore students are advised to watch the hands on video prior to come to class. Attendance is NOT optional. Individual participation is also required. There will be no make-ups for missed midterm or assignments, unless any special arrangements is made with the instructor beforehand.
- All student must complete the Syllabus agreement through Canvas quiz by Aug 26, 2014 11:59 pm. Any one failed to do so will be dropped from the class.
- There will be 3 home works and 3 individual projects, one midterm and final exam. All home works and projects should be submitted through Canvas. No scanned copy of handwritten solution is allowed. Allowed document types are PDF / ODT / DOC.

Project report should contain the following.
- Introduction containing objective.
- Requirement.
- Design and Implementation.
- Testing
- Conclusion
- Make sure to
  1. Include clear diagrams for requirement and design.
  2. Include code snippet to explain implementation.
  3. Include screen shots of testing waveforms and results.
  4. Upload HDL source code and test program as zip archive.

Project reports are encouraged to be submitted in IEEE format, [ http://www.ieee.org/conferences_events/conferences/publishing/templates.html ]
10% of the obtained marks will be awarded as extra points in project evaluation if report submitted in proper IEEE format.

NOTE that University policy F69-24 at http://www.sjsu.edu/senate/docs/F69-24.pdf states that “Students should attend all meetings of their classes, not only because they are responsible for material discussed therein, but because active participation is frequently essential to insure maximum benefit for all members of the class. Attendance per se shall not be used as a criterion for grading.”

Grading Policy

1. Homework carries 30% towards final score. Average of 3 score from homework will be contributed.
2. Project carries 30% towards final score. Average of 3 score from projects will be contributed.
3. Midterm carries 20% towards final score.
4. Final carries 20% towards final score.

Submission is allowed till **11:59 pm on due date**. Zero delay tolerance for the submission, i.e. NO late submission is permitted, unless you make special arrangements with your instructor beforehand.

You will receive a numeric score for the midterm, the final, each of the total homework, and each project submission. Letter grade, which is your class grade, will be obtained by adding the numeric scores and weighing with the percentages given below. Fraction in percentage will be converted into nearest integer value (‘> = 0.5’ will be moved to next integer number, ‘< 0.5’ will be moved to previous integer number).

<table>
<thead>
<tr>
<th>Grade</th>
<th>Percentage Range</th>
<th>Grade</th>
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<th>Grade</th>
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<tbody>
<tr>
<td>A+</td>
<td>100-97%</td>
<td>A-</td>
<td>92-90%</td>
<td>A-</td>
<td>92-90%</td>
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<tr>
<td>B+</td>
<td>89-87%</td>
<td>B-</td>
<td>82-80%</td>
<td>B-</td>
<td>82-80%</td>
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<tr>
<td>C+</td>
<td>79-77%</td>
<td>C-</td>
<td>72-70%</td>
<td>C-</td>
<td>72-70%</td>
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<tr>
<td>D+</td>
<td>69-67%</td>
<td>D-</td>
<td>62-60%</td>
<td>D-</td>
<td>62-60%</td>
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<tr>
<td>F</td>
<td>59-0%</td>
<td>Failure</td>
<td>59-0%</td>
<td>Failure</td>
<td>59-0%</td>
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</tbody>
</table>

Note that “All students have the right, within a reasonable time, to know their academic scores, to review their grade-dependent work, and to be provided with explanations for the determination of their course grades.” See University Policy F13-1 at http://www.sjsu.edu/senate/docs/F13-1.pdf for more details.
Classroom Protocol

1. **You must come to class on time!** Students entering the classroom late disrupt the lecture and/or the students already in class who may be engaged in lab or discussion. Late students will not be accepted in class.

2. If you miss a lecture you are still responsible for any material discussed or assignments given. A large portion of each class will be used for hands-on lab/discussion. All students are expected to participate in class activities. Students who are often absent will find themselves at a disadvantage during the tests.

3. No audio/video recording or photography in the classroom without prior permission of instructor.

4. No personal discussion or cell phone activity during class time. Please set the cell phone on silent/vibrate mode.

5. All e-mail communication to the instructor must have the subject line start with [CS-147, 03]

6. Email to be sent to the instructor's SJSU email ID (kaushik.patra@sjsu.edu) only.

University Policies

**General Expectations, Rights and Responsibilities of the Student**

As members of the academic community, students accept both the rights and responsibilities incumbent upon all members of the institution. Students are encouraged to familiarize themselves with SJSU’s policies and practices pertaining to the procedures to follow if and when questions or concerns about a class arises. See University Policy S90–5 at http://www.sjsu.edu/senate/docs/S90-5.pdf. More detailed information on a variety of related topics is available in the SJSU catalog, at http://info.sjsu.edu/web-dbgen/narr/catalog/rec-12234.12506.html. In general, it is recommended that students begin by seeking clarification or discussing concerns with their instructor. If such conversation is not possible, or if it does not serve to address the issue, it is recommended that the student contact the Department Chair as a next step.

**Dropping and Adding**

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester’s Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic year calendars document on the Academic Calendars webpage at http://www.sjsu.edu/provost/services/academic_calendars/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/. Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

**Consent for Recording of Class and Public Sharing of Instructor Material**

University Policy S12-7, http://www.sjsu.edu/senate/docs/S12-7.pdf, requires students to obtain instructor’s permission to record the course and the following items to be included in the syllabus:

- “Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor’s permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material.”
It is suggested that the greensheet include the instructor’s process for granting permission, whether in writing or orally and whether for the whole semester or on a class by class basis.

In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.

- “Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent.”

**Academic integrity**

Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The [University Academic Integrity Policy S07-2](http://www.sjsu.edu/senate/docs/S07-2.pdf) requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The [Student Conduct and Ethical Development website](http://www.sjsu.edu/studentconduct/) is available at [http://www.sjsu.edu/senate/docs/S07-2.pdf](http://www.sjsu.edu/senate/docs/S07-2.pdf).

**Campus Policy in Compliance with the American Disabilities Act**

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. [Presidential Directive 97-03](http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf) requires that students with disabilities requesting accommodations must register with the [Accessible Education Center (AEC)](http://www.sjsu.edu/aec) to establish a record of their disability.

**Accommodation to Students' Religious Holidays**

San José State University shall provide accommodation on any graded class work or activities for students wishing to observe religious holidays when such observances require students to be absent from class. It is the responsibility of the student to inform the instructor, in writing, about such holidays before the add deadline at the start of each semester. If such holidays occur before the add deadline, the student must notify the instructor, in writing, at least three days before the date that he/she will be absent. It is the responsibility of the instructor to make every reasonable effort to honor the student request without penalty, and of the student to make up the work missed. See [University Policy S14-7](http://www.sjsu.edu/senate/docs/S14-7.pdf).

**Student Technology Resources**

Computer labs for student use are available in the [Academic Success Center](http://www.sjsu.edu/at/asc/) located on the 1st floor of Clark Hall and in the Associated Students Lab on the 2nd floor of the Student Union. Additional computer labs may be available in your department/college. Computers are also available in the Martin Luther King Library. A wide variety of audio-visual equipment is available for student checkout from Media Services located in IRC 112. These items include DV and HD digital camcorders; digital still cameras; video, slide and overhead projectors; DVD, CD, and audiotape players; sound systems, wireless microphones, projection screens and monitors.
### Course Schedule – subject to change by instructor with due notice.

<table>
<thead>
<tr>
<th>Date</th>
<th>Lecture</th>
<th>Lab</th>
<th>Notes</th>
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<tbody>
<tr>
<td>08/24/15</td>
<td>Intro CS147</td>
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<tr>
<td>08/26/15</td>
<td>Introduction to Computer, Basic Instruction Set, ALU Tool setup</td>
<td></td>
<td>HW01 Posted</td>
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<td></td>
<td>Project I Posted</td>
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<td>Submit Prerequisite Survey &amp; Syllabus Agreement</td>
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<tr>
<td>08/31/15</td>
<td>Clock, Memory, Controller, Von-Neumann Architecture, System Software</td>
<td>Simulation Project</td>
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<tr>
<td>09/02/15</td>
<td>Digital Synthesis, Number Representation Hierarchical Models</td>
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<td>Add code will be supplied through e-mail</td>
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<tr>
<td>09/07/15</td>
<td><strong>Labor Day – Campus Closed</strong></td>
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<tr>
<td>09/09/15</td>
<td>Boolean Algebra I Data Flow Modeling I</td>
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<tr>
<td>09/14/15</td>
<td>Boolean Algebra II Data Flow Modeling II Project II Posted</td>
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<tr>
<td>09/16/15</td>
<td>Comb/Seq Logic I Memory Modeling HW02 Posted</td>
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<tr>
<td>09/21/15</td>
<td>Comb/Seq Logic II Project 02 Discussion Project I Submission</td>
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<tr>
<td>09/23/15</td>
<td>Seq Logic Design, Common Digital Components I Behavioral Modeling I</td>
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<td>HW01 Submission</td>
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<tr>
<td>09/28/15</td>
<td>Common Digital Components II Behavioral Modeling II Project 02 Milestone 1 Submission</td>
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<tr>
<td>09/30/15</td>
<td>Addition / Subtraction Logic Circuit Behavioral Modeling III</td>
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<tr>
<td>10/05/15</td>
<td>Multiplication Logic Circuit Behavioral Modeling IV Project 02 Milestone 2 Submission</td>
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<td>10/07/15</td>
<td>Division Logic Circuit Project 02</td>
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<tr>
<td>10/12/15</td>
<td>Putting Together a Microprocessor Project 02 Project 02 Milestone 3 Submission</td>
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<tr>
<td>10/14/15</td>
<td><strong>Midterm Exam</strong></td>
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<tr>
<td>10/19/15</td>
<td>Instruction Set Architecture, RISC/CISC Project 02 Project 02 Milestone 4 Submission</td>
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<tr>
<td>10/21/15</td>
<td>Processor Performance Measurement Project 02 Project III Posted</td>
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<tr>
<td>10/26/15</td>
<td>Pipeline Architecture I Gate Level Modeling I Project II Submission</td>
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<tr>
<td>10/28/15</td>
<td>Pipeline Architecture II Gate Level Modeling II</td>
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<tr>
<td>Date</td>
<td>Topic</td>
<td>Project</td>
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<tr>
<td>11/02/15</td>
<td>ILP, Hardware Threading</td>
<td>Gate Level Modeling II</td>
<td>HW03 Posted</td>
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<td>11/04/15</td>
<td>Parallel Processing I</td>
<td>Project 03 Part I</td>
<td>HW02 Submission</td>
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<tr>
<td>11/09/15</td>
<td>Parallel Processing II</td>
<td>Project 03 Part II</td>
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<tr>
<td>11/11/15</td>
<td>Veteran's Day – Campus Closed</td>
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<tr>
<td>11/16/15</td>
<td>Memory Hierarchy, Cache Memory I</td>
<td>Project 03 Part III</td>
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<tr>
<td>11/18/15</td>
<td>Cache Memory II</td>
<td>Project 03 Part IV</td>
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<tr>
<td>11/23/15</td>
<td>Cache Memory III</td>
<td>Project 03 Part V</td>
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<tr>
<td>11/25/15</td>
<td>Cache Memory IV</td>
<td>Project 03 Part VI</td>
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<tr>
<td>11/30/15</td>
<td>Virtual Memory</td>
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<tr>
<td>12/02/15</td>
<td>Review I</td>
<td></td>
<td>HW03 Submission</td>
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<tr>
<td>12/07/15</td>
<td>Review II</td>
<td></td>
<td>Project III Submission</td>
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<tr>
<td>12/14/15</td>
<td>Final Exam @ 7:45 PM – 10:00 PM (MH223)</td>
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