EFFECT OF LATTICE DAMAGE AND TED IN ULTRA SHALLOW JUNCTION FORMATION OF MOSFET USING ION IMPLANTATION

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December 4th, 2002

In partial fulfillment of course requirement for MatE 115, Fall 2002

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1.0 Introduction

The invention of the transistor initiated the electronic revolution of the 20th century[1]. MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor. Liandrat first proposed in 1935 that the conductivity of a surface region in a semiconductor could be modulated by the application of a perpendicular electric field[2]. This is known as “field effect” concept. In December 1947, three researchers from Bell Labs: J. Bardeen, W. Brattain, and W. Shockley, developed point contact transistors based on field effect theory[2]. In 1948, Shockley formulated his p-n junction theory to support the transistor effect observed by Bardeen and Brattain[2]. The NPN junction transistor or BJT (Bipolar Junction Transistor) was commercially available by mid 1950s[2]. Invention of integrated circuit occurred in 1959 and was due to J. Kilby of Texas Instruments and R. Noyce of Fairchild Semiconductor[2]. In 1959, M. Atalla and coworkers in Bell Labs demonstrated reduced surface effects of the grown oxide on silicon. This work of Atalla on controlling surface states led to the fabrication of the first MOSFET in 1960[1]. But MOSFETS started to become popular in the early 1970s[1].

MOSFETS are used in every electronic circuit. The products based on these devices have improved our lives in every aspect, starting from communication and education to transportation and recreation.

This paper provides a basic understanding of ion implantation mechanisms and the cause

of lattice damage produced by it. This is followed by a discussion of the effects of damage repair techniques, such as annealing, on the defects. The relationship between the defects and transient enhanced diffusion phenomenon is also included. Rapid Thermal Annealing and Plasma Based Ion Implantation are briefly described which are used to fabricate shallow junction and control TED(Transient Enhanced Diffusion). Next the dimensions of the shallow source drain junction are briefly discussed and a relationship between the junction depth and electrical properties of the MOSFET is explained.

2.0 Ion Implantation Mechanisms

Ion beam of the species to be implanted is created by an ion source. The ions are accelerated in a vacuum chamber through a potential of tens to hundreds of kilovolts[3]. When this high energy ions hit the silicon wafers, it causes displacement of silicon atoms. The amount and range of implanted ions can be accurately controlled and modeled. Since each ion carries a fixed and known charge, the beam current intensity is a direct and accurate measure of the number of the ions deposited. To increase the dose requires a longer implant time or higher beam current[4].

The implanted dopant distribution can be modeled statistically and is often modeled to the first order by a symmetric Gaussian distribution.

$$C(x) = C_p \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p}\right) \qquad \text{Equation 1}$$

In Equation 1, R_p is the average projected range, ΔR_p is the standard deviation about the range and C_p is the peak concentration where the Gaussian is centered[4].

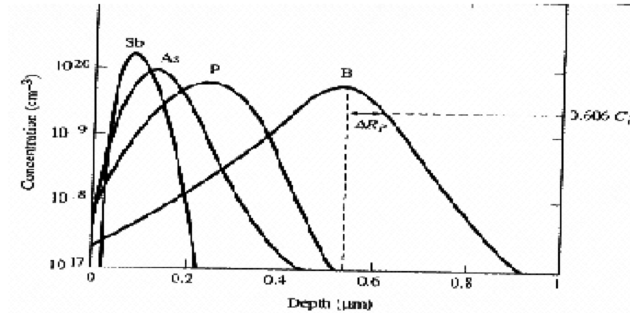

Figure 1. Distribution of ions into crystalline silicon at an energy of 200 keV.[4]

Figure 1 shows the distribution of ions implanted into the crystalline silicon. The lighter ions show a higher standard deviation from the projected range than that of the heavier atoms.

2.1 Lattice Damage by Ion Implantation

In crystalline silicon, the trajectory of an implanted ion depends on structure of the lattice after the ion is set in motion[5]. The implanted ion loses energy by both nuclear and electronic stopping offered by the target. Nuclear stopping is due to the energy loss resulting from collision with target atoms. The electronic stopping is due to the drag force

exerted on the moving ion in the dielectric medium[5]. Nuclear stopping dominates towards the end of the trajectory, when the energy of the implanted ion becomes less[5]. This helps creating a high degree damage in the lattice. Fifteen eV energy is required to displace a silicon atom from its lattice site to create a stable separated interstitial and vacancy(a Frenkel Pair)[5]. Since implant energy is in the range of keV, a large number of displacement is produced[5]. For heavier atoms, like arsenic, the stopping is dominated by nuclear stopping. So the damage is evenly spread over the whole range of the trajectory of the implant ion[5]. For lighter ions, such as boron, the high energy stopping is dominated by electronic stopping. So the damage is clustered at the end of the trajectory where energy is less and stopping is dominated by nuclear stopping mechanism[5].

2.2 Damage repair by annealing

The implanted dopant atom requires restoration. Damage annealing is carried out to restore the implanted atoms in the substitutional sites and repair the broken bonds of the Si lattice. The extended defects, formed in projected range region are well known to be {113} defects as stated by Aditya et. al.[6] By TEM investigation, it has been shown that these defects lie on {113} planes and are elongated in <110> direction[4]. Upon annealing the defects grow in size and decrease in density[8].

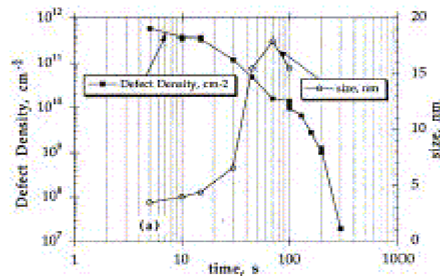

Figure 2. Density and size evolution of a population of {113} defects after annealing at 815°C [7]

After a 1-3 second anneal at 600°C-800°C, the defects grow in concentration. After increasing the temperature further, the defects starts to dissolve, as found in the results of an experiment by Giovanni et. al.[8]. But if the damage is above the critical level, some of the {113} defects form stable dislocation loop. These loops are known as End of Range (EOR) defects as described by A. Claverie et. al.[7] At about 1000°C, these loops ripens to form energetically favorable bigger loops, without releasing the interstitials. This dislocation loops will disappear at even higher temperature, at 1100°C after annealing for 60 seconds.[7]

2.4 Transient Enhanced Diffusion (TED) and Rapid Thermal Annealing (RTA)

Higher temperature annealing causes another effect in the implanted profile which is known as transient enhanced diffusion (TED). Especially low energy implant (for boron) profiles show a time dependent diffusion phenomenon which changes the tail of the profile. This diffusion phenomenon is, as stated by A. Claverie et. al.[7],

1. Transient i.e., its amplitude decreases with time

2. Depth dependent i.e., its amplitude depends on the distances between the defects, boron and the surface.
3. Enhanced, in the case of boron, by sometimes orders of magnitude with respect to 'normal' diffusion observed for longer annealing durations.

TED of dopant impurities in silicon during annealing of ion implantation damage is driven by the time dependent evolution of the damage into clusters and extended defects as discussed earlier[8]. In order to form a shallow junction, the implant energy is lowered to achieve a reduced projected range, Rp. However, TED significantly alters the shallow junction profile at low energy implant.

Most of the damage due to implantation is removed during the early stage of annealing by defect recombination[6]. This leaves excess interstitials which are approximately equal in number to the implanted dose. This excess interstitials are then trapped into metastable extended defects[6]. As stated by N.E.B Cowern et. al., it is now generally agreed that these defects, trapping large number of interstitials, are relatively unstable at high temperature[8]. So they cause a diffusion enhancement at high temperature annealing over a small period of time.

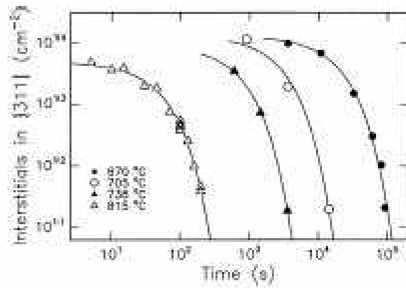

Figure 3(a)

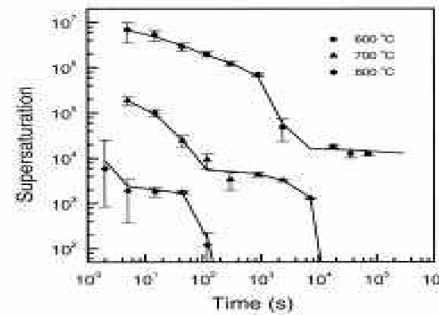

Figure 3(b)

Figure 3(a). Evolution of total number of Si interstitials bound to the {113} defects upon annealing at various temperature[7].

Figure 3(b). Interstitial supersaturation plotted as a function of annealing time and temperature[8].

Figure 3(a) shows that the total number of Si atoms bound to the defects which decreases as the anneal proceeds. So the rate of release of Si atoms from defect rich regions increases with increasing temperature. So for higher temperature the whole defect region releases Si atoms which diffuses towards bulk and surface region[8]. N.E.B Cowern et. al. presented a methodology to model the interstitial saturation as a function of time and anneal temperature which is shown in Figure 3(b). The model also suggests that at higher temperature annealing, the rate of decrease of interstitial saturation is higher than that at low temperature annealing[8]. And the data also indicate two phases of TED. An initial phase of ultra fast TED is followed by 'plateau' of near constant rate[8]. After some time, the diffusion rate is again higher. This data indicates the time dependence of the {311} defect evolution. The plateau is because of the time taken by the {311} defects to form

stable loops. After sometime, they start to dissolve contributing to the TED[8].

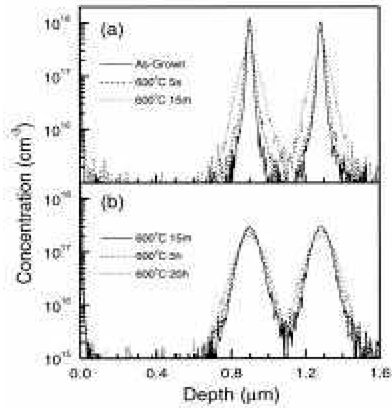

Figure 4. Time dependence of TED for boron. Annealing at 600°C for different range of times.(from Ref. [3])

Figure 4. shows the SIMS (secondary-ion mass spectrometry) profile of a boron implantation on Si wafer with 40 keV. The samples were annealed at 600°C for times in the range of 1 second to 20 hours[6]. This experiment was done by N.E.B Cowern et al.[8]. Significant diffusion occurs within first seconds of annealing (5 seconds – 15 mins) which indicates a huge supersaturation of interstitials (in the order of 10^7). After that, much less diffusion occurs during the period 15min-20 hours, indicating a large drop in supersatuartion[8].

As TED alters the implanted profile, it is very difficult to control the implant concentration at projected depth after annealing. This poses the biggest challenge to the formation of shallow junction of the submicron MOSFETS. Low energy, high dose ion implantation is required to form shallow junctions with low sheet resistivity[8]. Since

TED is a dominant phenomenon for low energy implantation, various methods are being used and developed to form shallow junctions. RTA (rapid thermal annealing) is a commonly used annealing technique which minimizes TED during thermal annealing by following a predefined anneal temperature profile (w.r.t time). Generally the specimen is annealed by applying a temperature ramp. After that the specimen is soaked in constant temperature for some time. A negative ramp anneal follows the “soak” period. There are other variations of RTA such as RTSA (rapid thermal spike anneal) also which is also used.

2.4 Plasma Immersion Ion Implantation (PIII or PBII)

Plasma based ion implantation (PBII) is now being considered as a promising technique for shallow junction formation for MOSFETS and large area doping in CMOS technology. In conventional ion beam implant, the low beam current lead to high cost for high dose implant. Low energy implants are limited by the ion beam optics when high doses are required[3]. PIII is well suited for these purpose because it can deliver high ion currents at low energies. Another advantage of PIII is that it can treat large area. Conventional ion beam implant is a line of sight process. The object requires manipulation for an implant in desired surface areas[3]. PIII technology is capable of doping with comparatively high concentration on large areas.

The sample or substrate is placed on a sample holder in a vacuum chamber. A pumping

system and a gas feed system is used to immerse the sample in the working gas at a suitable pressure. Then Plasma is generated in the vacuum chamber which envelopes the sample[9]. The sample is negatively biased.

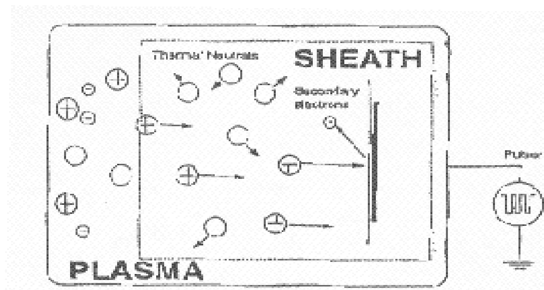

Figure 5. Schematic drawing of PIII technology [9]

Electrons are repelled away from the sample or wafer and a sheath region of positive ions is established around the wafer holder. Positive ions inside the sheath region is attracted by the negative potential of the target and accelerate toward it. The ions gather kinetic energy while traversing the sheath and implant at energies up to the potential difference of the sheath[9].

W. Easinger summarized the results from different experiments of p+/n+ doping using PIII in his paper[9]. In 1993 Felch et al., and in 1994 Shung et al. could achieve 80-130 nm junction depth for boron implant[9]. Doping concentration at a certain depth is dependent on the bias voltage. In 1995 Felch et al found junction depths of 55 nm for 1 kV bias and 35 nm at 0.75 kV bias. The sheet resistance of such a wafer was reported to be 294 ohm/square[9]. At the same time Qin et al. could achieve sheet resistance as low

as 42 ohm/square[9].

In 1995 Mizuno et al. reported n^+ doping with As. At a depth of 50 nm, the concentration was decreased by four order of magnitude[9]. Kakinuma et al. also reported n^+ doping with phosphorus. They also observed that concentration decreases by four order of magnitude at 50-100nm depth[9]. These examples from different laboratories using different plasma generation and process parameters demonstrate the feasibility of p^+/n^+ doping of silicon is possible by PIII and leads good results[9].

3.0 Application in Junction Formation

The drain and source regions are formed by ion implantation. Formation of drain/source region is carried out in different steps. The most commonly used source and drain structure in todays MOSFETS is lightly doped drain (LDD) structure. To overcome the hot carrier effect resulting from increasing electric field in scaled devices, the graded doping profile is used for drain/source region of MOSFET. This helps the drain voltage to drop over a large distance. For a P channel MOSFET, p^+ diffusion is required for source/drain regions. But instead of an abrupt p^+n junction, p^+p^-n is created between drain/source and channel. The p^- region is the lightly doped extended region of the drain source region.

As the MOS device are approaching 0.1 μm regime, the drain/source junctions get shallower to about sub 50 nm in depth[10].

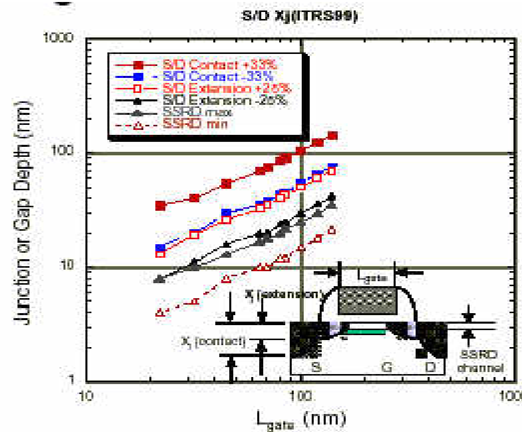

Figure 7. Guiding equations of SD junction depths presented in ITRS99[10].

Figure 7. shows the empirical relationship between the scaling of S/D junction depths and the scaling of transistor channel length. The contact area source/drain junction depth follows the equation; x_j (contact)= $0.8*L_{gate}$ +/- 33%. The scaling of source/drain extension (SDE) is shown to be x_j(extension)=$0.4*L_{gate}$ +/- 25% and SSRD (Super Steep Retrograde Doped) channel depth is scaled with gate dimension ($0.2*L_{gate}$)[10]. SDE (Source Drain Extension) connects the SSRD channel with the deep source/drain of contact area. Junction depths of the SDE region are currently 40-60 nm for 0.13 μm MOSFETS and are predicted to be as low as 10nm for future deep submicron devices[11]. The parasitic resistance of the SDE area is the dominant component that limit the drive current of the channel. As the channel length or transistor as well as the SDE junction depth is scaled, the sheet resistance value of the SDE area is becoming a limiting factor of the scaling. According to ITRS01 (International Technology Roadmap for Semiconductors) report, dopant activation for low energy implant and spike RTP

(1050C/1s) could achieve sheet resistance of 10^{-3} ohms-cm, which is close to the maximum value of the desirable sheet resistance of the SDE junction[10]. By varying the implant energy and RTA temperature, the SDE junction depth can be controlled for an optimum parasitic resistance value which provides the desired drive current of the transistor. This ultra shallow junction in modern MOSFETS can be fabricated by various well researched ion implantation techniques to obtain high dose (to reduce parasitic resistance) and low energy (shallow implant) implantation where the effect of TED is carefully controlled. Methods of reducing TED include lowering implant energies, amorphization followed by solid phase epitaxial regrowth and high temperature, and short time RTA cycles[11].

5.0 Conclusion

In order to increase switching speed and decrease power dissipation, length of MOSFET are being continuously scaled down. To keep pace with this scaling of minimum feature size, ability to fabricate ultra shallow SDE junctions has to be developed. PBII is being considered as a possible alternative for high dose low energy implant. This paper discussed the present issues of using conventional ion implantation for low energy high dose implantation.

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