

The Application of Carbon Nanotubes in Field Effect Transistors

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Dec.2nd 2002

Submitted in partial fulfillment of course requirements for MatE 115 Fall 2002.

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1.0 Introduction

When it comes to the determination of the origins of Carbon Nanotubes, there is still some debate within the scientific community. Interest seems to have developed out of research into the production of carbon fibers for composite materials over the last century⁽¹⁾. In 1991, Sumio Iijima of Japan used a high-resolution TEM (transmission electron microscopy) to observe carbon nanotubes directly⁽²⁾. Mr. Iijima recognized that the filament like objects he was observing in a pile of carbon soot had an orderly and structured arrangement. He then used electron diffraction analysis to show that the crystal axis of the graphene sheets in some of the tubes had a helical arrangement relative to the tube axis. These tube structures he later termed multi-walled nanotubes (MWNT)⁽³⁾. In the decade that has passed, the study of carbon nanotubes is in the process of transitioning from the research phase to the engineering phase. Those technologies, in which they can be applied most readily, are now being developed and in the case of field effect transistors, are currently being studied and characterized.

For some time now there has been much speculation on the longevity of data storage devices produced from silicon based integrated circuits. Higher storage density has meant increased device performance and for this reason has become the holy grail of device evolution. The problem here has been that the smaller the device dimensions, the more sophisticated the production equipment has become and subsequently, the higher the fabrication facility and capital equipment costs. Even though IC dimensions have shrunk continually, it has long been predicted that silicon based FET's will eventually be limited by photolithographic manufacturing methods, materials, and design issues. To date, with

silicon based FETs, “Prototype transistors with gate lengths in the 30-nm range have been successfully fabricated and were found to have excellent electrical characteristics ⁽⁴⁾.” This contrasts with carbon nanotubes whose diameters can range from a tenth of a nanometer up to several nanometers and whose lengths can be varied through fabrication methods. With dimensions on this level, nanoscale technologies hold the potential for storage densities that are orders of magnitude greater than those of silicon-based transistors. Although operational characteristics are still under study, prototype research devices have attained performance levels that compare with the best silicon FETs currently under development.

As more research and development efforts go into Carbon nanotube projects, upgrades to existing technologies, in addition to technological innovation, will begin to become apparent. These improvements will become evident in many ways, among which include faster data processing speeds for computers, more compact high performance communication devices, and increasingly sophisticated electronic equipment. Even at this time venture capital is being provided to scientist and engineers who are forming new companies while some of the large corporations are investing heavily in the field. With all of these efforts being directed toward nanoscale-based technology, it will be only a short period of time before they see widespread use in all forms of computers and electronics.

2.0 Description/Fabrication methods

Carbon nanotubes can be described as a monolayer sheet of graphite atoms arranged in a hexagonal grid pattern, that have been rolled into a tube. They can have a single wall, single cylinder tube (SWNT) or can have tubes of varying diameter within tubes, as in the case of multi-walled nanotubes (MWNT). Although most methods of production produce multi-walled tubes, single-walled tubes can be preferentially produced through the addition of a catalyst in the fabrication process. The graphene grid structure can either align itself with or it can twist with respect to the tube axis. This variation in alignment of the grid, in addition to the tube diameter, determines the electrical properties that different types of tubes will display. The more fundamental of which is whether the tube will behave as a metal or as a semiconductor.

Although there are a wide variety of research projects into the synthesis of carbon nanotubes, they have generally developed into three methods that are summarized in table 1. These include production from a high voltage spark across carbon rods, through chemical vapor deposition (CVD), or from a high temperature Laser beam pulse ⁽²⁾. Each method has its advantages and the processes that employ them are specific to the kind of application that the product tubes will be used for. In the case of tubes used in transistor research, CVD appears to be the method of choice.

If carbon rods are used, they are connected to a power supply and then placed a few millimeters apart in a mounting bracket. A high current is sent through the circuit producing a spark between the rods. The rods are consumed in the process and carbon

nanotubes are produced as a byproduct. If a catalyst is added to the carbon rods, the process will produce both single and multi-walled tubes of high purity, although short in length. Tubes produced through CVD are usually grown in a furnace reactor in which a carbon source gas has been introduced. As the gas decomposes at the elevated temperatures, the carbon will recombine into single or multi-walled nanotubes, depending on the catalyst used in the reaction. The advantage of CVD is the high level of process control and a wide variety of catalyst options. It also has an advantage in the control of tube length and selective positioning through either catalyst control or applied magnetic fields. The problem is that it is prone to defect incorporation into the grid structure during synthesis.

Table 1: Summary of Nanotube Production Processes.

Method	Description	Advantages/ Disadvantages
High Voltage Spark	High voltage/current spark across carbon rods.	Yield up to 30% by wt. Catalyst can be added to carbon rods for SWNT and MWNT production. High purity. Short in length.
Chemical Vapor Deposition	Vapor phase reaction of carbon source gas.	Produces mostly MWNT's. High yield, 20% to 100%. Controllable process. Long lengths possible. Prone to defect incorporation.
High Energy Laser Beam	Laser beam pulse onto carbon target, tubes result from carbon gas produced during laser pulse.	Good process control. Can use catalyst as backfill gas or in carbon source. Yields up to 70%. Produces narrow, predictable range of tube diameters. High equipment costs.

The third method uses a laser beam to vaporize a graphite target producing tubes from the resulting carbon gas. This method also allows for a good level of process control through regulation of the beam intensity, providing precise temperature control of the reaction. It also allows for the use of a catalyst making it the process of choice for the production of single-walled nanotubes. An advantage of the reaction temperature control is that it will produce a narrower range of tube diameters. The only drawback is the high cost associated with the lasers required to produce the reaction ⁽²⁾.

At this point, the production of carbon nanotubes is a somewhat random process. What is statistically controllable is whether a single or multi-walled tube is produced, its length, and to some degree, its orientation on a substrate. There is no control over the structural aspects of the tube, that is, they cannot control the diameter or the twist in tube growth. Therefore, a set of process conditions are developed that will produce a statistical distribution of tubes with the characteristics required. As an example, if single-walled, small diameter nanotubes are required, then the process conditions are set such that a narrow, Gaussian distribution of this kind of tubes will be produced even though it may also produce some multi-walled or large diameter tubes ⁽⁵⁾. Sometimes post fabrication treatments are employed that reduce the numbers of unwanted tube morphologies through selective oxidation treatments or chemical screening methods ⁽⁶⁾. If the process conditions are set properly, in addition to chemical pretreatments, tubes of selective diameters will burn up in the oxidation process leaving a tube population with a narrow distribution of tube diameters.

Methods such as these are being studied as a means of narrowing the kind of tube required for a specific application, but the ability to construct tubes with a particular set of requirements is not yet possible.

Nanotube manipulation and alignment is another critical issue for the development of nanotube-based integrated circuits. In order to compete with the densities being produced with silicon integrated circuits, manufacturing methods will have to be developed in which large amounts of tubes with specific properties can be grown in specific locations. For this purpose, catalysts are being used to select for growth of single-walled or multi-walled tubes and for selective orientation of tube growth on substrates. The goal in this case being to grow nanotubes in specific locations as required by the design of the electronic component. In the case of catalysts for electronic applications, cobalt and molybdenum are examples of materials being studied in combination with CVD process methods. One interesting approach is being developed by a group of researchers in Korea using PVD deposited films. Thin cobalt and cobalt-molybdenum films (between 10Å and 100Å) are deposited onto a silicon substrate, heated at high temperature in a reaction furnace (~900°C) to allow for film agglomeration into distinct particle islands, and then exposed to different kinds of carbon source gases⁽⁷⁾. The particle islands behave as a kind of nucleation site for nanotube growth and depending on the characteristics of the particle, will produce tubes with a distinct morphology in a specific location. Although this project presents a novel approach, it represents the fundamental stage that fabrication engineering is at. There is still a good deal of research to be done before highly integrated, nanotube-based transistor arrays can be produced.

3.0 Principle / Mechanism

With the production of CNT's has come the analysis and characterization of their physical, mechanical, and electrical properties. The factors that contribute to these properties are extremely complex and in many cases theoretical. A thorough treatment of the theory involved is extremely complex and beyond the scope of this paper. What follows is an intuitive explanation based on generally accepted findings that have been condensed and presented in their most basic form.

Classification of CNT's has fallen into three categories based on the way that the tube wraps itself with respect to the tube axis. These categories are referred to as Armchair, Zigzag, and Chiral ⁽¹⁾. Figure-1 below depicts graphically how each of the three types of nanotubes can be distinguished from an overlay of a set of vectors drawn onto a graphene sheet.

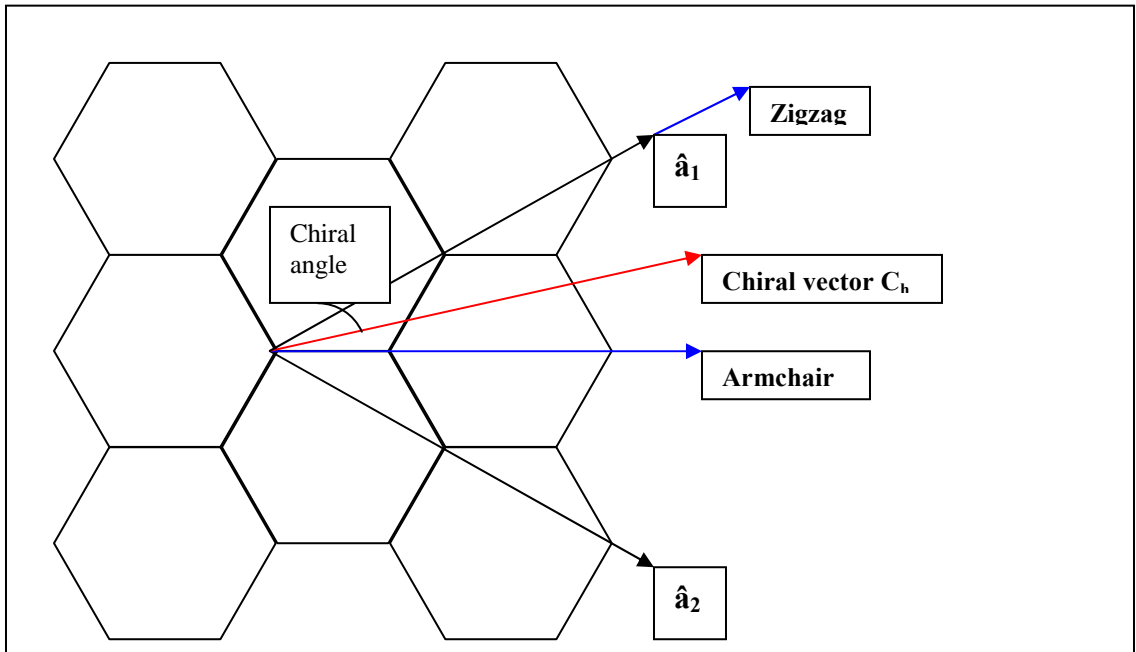


Figure-1: Nanotube Chirality Diagram.

Whether a nanotube meets one of the three classifications is dependent on the magnitude of the Chiral vector and the angle it makes with unit vector \hat{a}_1 . The magnitude will determine the tube circumference and the angle will determine the degree of twist. Equation 1 is often used to demonstrate the magnitude of the chiral vector where \hat{a}_1 and \hat{a}_2 are unit vectors and n and m are integer coefficients. If the values of n and m are varied then the magnitude of the chiral vector and the angle it makes with respect to unit vector \hat{a}_1 will vary.

$$\mathbf{Ch} = n\hat{a}_1 + m\hat{a}_2 \quad \text{Equation 1}$$

Once the magnitude is known, the diameter of the tube can be roughly determined by taking the magnitude times 0.25. Or more specifically, the tube diameter can be determined if n and m are known in addition to the carbon to carbon atom distance a_{c-c} , by means of the Equation 2.

$$Dt = (\sqrt{3}/\pi) a_{c-c} (m^2 + mn + n^2)^{1/2} \quad \text{Equation 2}$$

With the value of Ch established, the angle that the chiral vector makes with unit vector \hat{a}_1 , the chiral angle, can be determined. By taking the values of n and m, the chiral angle can be determined from Equation 3.

$$\text{Angle } \theta = \tan^{-1}(\sqrt{3n/2m+n}) \quad \text{Equation 3}$$

As demonstrated in determining the characteristics of the chiral vector, integer coefficients n and m are of major importance in determining the key elements of the nanotube structure. When both ends of the chiral vector meet they form the circumference of the tube.

Therefore, different values of n and m will give different magnitudes of the chiral vector, different tube diameters, different chiral angles, and as a result, different degrees of twist to the tube. The following table summarizes these effects on tube morphology.

Table 2: Effect of Integer Coefficients on Tube Morphology.

Type	Integer Coefficients	Chiral angle	Morphology
Armchair	$n = m$	30°	No twist wrt tube axis
Zigzag	$n = 0$ or $m = 0$	0°	Maximum twist angle
Chiral	Both n and m vary in value.	Angle varies between 0° and 30° .	Twist angle between no twist and maximum twist.

The properties of carbon nanotubes are influenced mostly through the diameter of the tube and its degree of twist. Both aligned tubes and tubes with a twist can be metallic or semiconducting but this will depend on whether the energy states in the circumferential direction pass through what is termed a Fermi point. At these Fermi point locations, the valence and conduction band meet and this allows for conduction in the circumferential direction of the tube. Tubes that have the correct combination of diameter and chirality will align with a set of Fermi points around the perimeter of their grid structures throughout the length of the tube. These tubes will show metallic like conduction. If the diameter and chirality do not meet at a set of Fermi points then the tubes will exhibit semiconducting behavior ⁽⁸⁾.

In addition to Fermi point matchups, the cylindrical shape and diameter of the tube affects electron transport through the way in which quantum states exist around the tube perimeter. Small diameter tubes will have a high circumferential band gap with a low

number of energy states available. But as the tube diameter increases, the number of energy states increases and the circumferential band gap decreases. In general, the band gap is inversely proportional to the tube diameter ⁽⁸⁾. In addition, the wave properties of electron behavior are such that standing waves can be set up radially around the tube. These standing waves and lack of conduction states in small diameter tubes, along with the monolayer thickness of the graphite sheet, tend to block electron motion around the tube perimeter and force electrons to be transported along the tube parallel to its axis ⁽¹⁾. This is if the small diameter tube does not have a Fermi point matchup. If a matchup is included then electron transport can occur around the tube perimeter, in addition to axial conduction, allowing for increased transport options of the electron and metallic conduction characteristics. As the tube diameter increases, more energy states are allowed around the tube perimeter and this also tends to lower the band gap. So when only axial conduction is allowed, the tube exhibits semiconducting behavior. When both axial and circumferential conduction are allowed, the tube exhibits metallic conduction.

4.0 Application

At this point, most of the research into carbon nanotube transistors is being conducted with what are known as hybrid devices. These are devices that combine CNT's with conventional silicon transistor technology. Hybrid devices are under study because they are easy to fabricate with existing manufacturing methods and the characteristics of silicon transistors are well characterized. The hybrid devices that are being reported on usually have a design in which the carbon nanotube acts in the same fashion as a channel of doped silicon in metal oxide semiconductor circuits (MOSFET). In MOSFET's, the channel is doped so that with the proper field applied to a gate electrode, a current can

flow through the transistor. This gate voltage sets up a field in which either electrons or holes (depending on how the channel is doped) are attracted to or are repelled away from the channel. If accumulation of either one takes place in the channel, then a current is allowed to flow between the source and drain junctions on either side of the channel. So by switching the gate voltage between values, current will flow or not flow through the transistor and this identifies it as being in an on or off state. Figure 2 identifies the essential elements of the MOSFET design for reference,

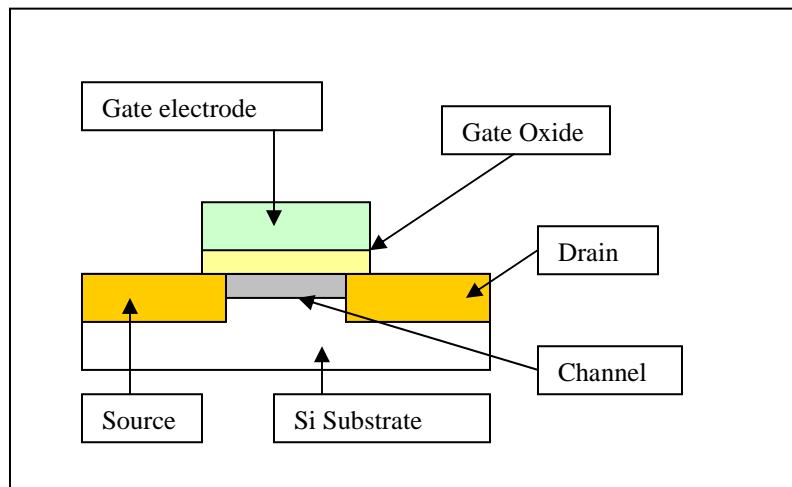


Figure 2: MOSFET Design Elements.

In the case of a hybrid carbon nanotube transistor, the nanotube acts as the channel. Most of the circuit designs have the tubes placed so as to span a gap between two gold electrodes. A typical design is shown in figure 3 where a doped silicon wafer acts as the substrate. It has a layer of silicon dioxide grown on top of it and on top of the SiO₂ a layer of gold is deposited and then formed into electrodes through photolithographic techniques. A carbon nanotube is then placed in contact with the electrodes, lying on top

of the SiO₂ layer, and spanning the space between the electrodes. Probes are placed on the electrodes to send current through the tube. Voltages are applied to the back of the wafer so as to set up a field with respect to the tube axis, a technique termed “backgating”. In this way current flow can be controlled through the tube depending on the voltage applied to the back of the wafer.

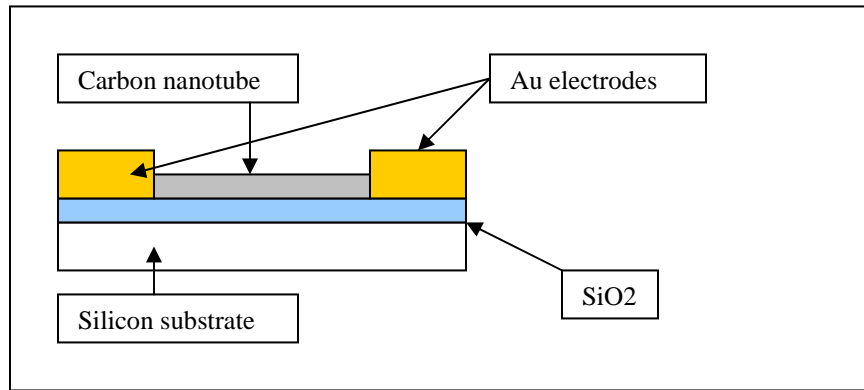


Figure 3: CNTFET Design Elements.

Simple hybrid transistors of this design have been fabricated and used to study the feasibility of carbon nanotubes as channel conductors in field effect transistors. Researchers at IBM have studied field effect characteristics on channel conduction in both single and multi-walled nanotubes. In transistors with single walled nanotubes, they were able to demonstrate linear current voltage characteristics between the source and drain electrodes with no voltage applied to the back of the wafer. The same test was then run with “gate” voltages applied ranging between negative 6 volts and positive 6 volts. The current voltage characteristics were measured through the tube for each of the voltages applied to the back of the wafer. They determined that negative “gate” voltages would allow linear current/voltage flow through the tube, but as the gate voltage became

more positive, the current dropped to zero. This indicated that the current transport mechanism through the tube was via hole migration rather than electrons, making the transistor behave like a p-type MOSFET. The effect of high positive back voltages was to drive holes away from the tube center and deplete it of a conduction mechanism ⁽⁹⁾. Further test were run to determine if the p-type behavior was a fundamental characteristic or not. It was determined that n-type behavior could be induced in p-type devices through a vacuum anneal process. This led to speculation that the initial p-type behavior was due to carrier injection at the nanotube gold electrode contact.

In addition to demonstrating field modulation effects in the nanotube, other properties such as hole density and mobility were studied. Although these results were encouraging, they really did not represent any substantial improvement over current MOSFET designs.

5.0 Summary / Conclusion

Presently, there is a vast array of resources and projects into carbon nanotube applications. These projects span a wide spectrum and the degree of progress being made is truly impressive. In the case of carbon nanotube transistors, hybrid devices are in the engineering phase but they have limitations and do not make the best use of their capabilities. Many believe that to make the best use of the scale and material properties, the devices will have to be fabricated and operated in nanoscale dimensions. This would mean semiconducting nanotubes acting as transistors and interconnection between them with metallic nanotubes. There are several obstacles that need to be overcome before any of this will take place. There will have to be some optimal form that a CNT memory

device will take. Obstacles include issues such as methods for growth and fabrication with the required properties, manipulation of objects on the molecular level both singularly and in mass, quality control issues where swings in critical parameters of five to ten percent can have an enormous effect on the performance of the device, and other issues of manufacture and cost control.

The most likely prospect is that carbon nanotubes will first be utilized in hybrid type devices. The problem with a hybrid device is that it will not be able to compete with silicon based CMOS technology in the near future. The main issue is that the field strength required to modulate channel conductance is area dependent and this imposes a limit to the integration scale that feature sizes can be reduced to. R. Stadler and M. Forshaw, at the University College in London, estimate that “Although device densities of 0.1 Mbit/cm² are realized, the authors (ref. 10) claim that 100 Mbit/cm² could be achieved. This would still not reach the densities that are expected for CMOS technology in the near future (475 Mbit/cm² for SRAM memories in 2006)”⁽¹⁰⁾. In the short term, the outlook would favor CMOS technology, but in the long term, as more progress is made in nanoscale technologies and these critical issues are resolved, nanoscale transistors and logic circuits will replace CMOS as the dominant form of integrated circuit design.

6.0 References

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