## The Electronic Scale

## Pre lab Questions

1. How many strain gages are there in the Wheatstone bridge circuit?
2. What is the purpose of the trim pot used in the Wheatstone bridge?
3. When adjusting the offset of the amplifier for the electronic scale, where should the offset be measured?

## Purpose

- To introduce operational amplifiers and their use in amplifying signal sources
- To configure, build, and test several common amplifier types.
- To learn how to interface an analog signal source to an A/D converter
- To build a digital electronic scale using strain gages, an amplifier, an A/D converter, and a microcontroller


## Components

| Qty. | Item |
| :---: | :--- |
| 1 | LF353 dual operational amplifier |
| 1 | ADC0831CCN 8 bit A/D converter |
| 1 | cantilever beam assembly with strain-gauges mounted on the top and bottom surfaces near <br> the base <br> 1 |
| 1 | 1 k resistor |
| 1 | 4.7 k resistor |
| 2 | $10 \mathrm{k} \Omega$ resistors |
| 2 | 200 k resistors |
| 1 | $1 \mathrm{k} \Omega$ trim pot |
| 1 | 100 k trim pot |
| 1 | $0.1 \mu \mathrm{~F}$ capacitor |
| 1 | $10 \mu \mathrm{~F}$ capacitor |

## Introduction

## The Devices

Figure 1 shows two common packages for operational amplifiers. The single package on the left contains one operational amplifier. The LF741 was one of the earliest IC op-amps and is still widely used. There are many varieties of op-amps available today. In this lab we will be dealing with opamps designed for small signal amplification. There are also power op-amps that are designed to source or sink relatively large currents at relatively high voltages. Small -signal single op-amp IC's are

[^0]usually pin-compatible with the ' 741 , but one should always check the data sheets to be sure. We will use the LF353 dual op-amp IC in this lab experiment. It contains two independent op-amps as shown. There are also quad-packages that contain 4 independent op-amps.

Op-amps are active devices, which means they must be powered in order to function. The typical configuration will use symmetrical positive and negative supply voltages $\left(\mathrm{V}_{\mathrm{S}}\right)$ in the range between $\pm 5$ V and $\pm 15 \mathrm{~V}$. There are some op-amps that are designed to work with single-sided supplies, i.e., where $-\mathrm{V}_{\mathrm{S}}$ is ground, and $+\mathrm{V}_{\mathrm{S}}$ is +5 V to +15 V .


Figure 1 Examples of single and dual op-amp IC packages. We will use the LF353 dual op-amp in this experiment.

## Procedure

1. Design and construct an inverting amplifier (see Figure 2) with a gain of -20 . Use a 10k resistor for R1. This will save you time later). Note the minus sign on the gain. The output polarity is inverted from the input. This is why it is called an "inverting amplifier." What must the resistance of R2 be? Set up the power supply for voltages of $\pm 12 \mathrm{~V}$ before connecting the power supply to the op-amp. Turn off the power supply before you wire it to the op-amp. It is always a good idea to do whatever wiring you need with all power to the circuit turned off.


Figure 2 An inverting amplifier. The gain of the amplifier is -R2/R1. It is always a good idea to keep the leads to the inputs of the op-amp and the feedback loop short to minimize noise pickup.

To test your circuit, first, set up the function generator with high $Z$ termination to output a $2 \mathbf{~ k H z}$ sine wave with an amplitude of 100 mV peak-to-peak (p-p). Check the output of the function generator with the 'scope first before you connect it to the amplifier. Then, connect the 'scope probe from Channel 1 to the input of your amplifier circuit, and the 'scope probe from Channel 2
to the output of the amplifier. Where should the ground clips of the scope probe be clipped? Before you attach the clips, turn to the last page to check your answer.

Now apply power to the circuit, and connect the function generator to the input of the amplifier. Compare the signals from Channel 1 and 2 displayed on the screen. Do the voltage peaks appear to be opposite each other? Does the amplitude of the output signal agree with your gain calculation? Increase the function generator amplitude until the op amp output appears to be chopped off at the peaks. At what input amplitude is the output clipped? Explain why this occurs.
2. Using the other op-amp on the LF353, construct a non-inverting amplifier with a gain of 50 as shown in Figure 3. Let $\mathrm{R} 1=1 \mathrm{k}$, and use a 100 k trim pot for R 2 . The gain of this circuit is (R1+R2)/R1.


Figure 3 A non-inverting amplifier. The gain of the amplifier is $1+\mathrm{R} 2 / \mathrm{R} 1$.
Test this circuit in the same manner as before, then input a 10 kHz square-wave with an amplitude of $0.5 \boldsymbol{V} \boldsymbol{p}-\boldsymbol{p}$. Compare the two signals displayed on the screen. Are the voltage peaks synchronized? With a square-wave, how would you tell if the voltage peaks were being chopped? Most importantly, what is the gain of this circuit?

## The Electronic Scale

3. Obtain a board with a cantilevered strain-gauge bracket from the instructor. These strain gauges convert mechanical strain into a proportional change in resistance. Here, we're going to incorporate the strain gauges into a circuit called a Wheatstone bridge as shown in Figure 4. Basically, a Wheatstone bridge uses four resistors, which are grouped into two pairs and connected to a voltage supply. The resistors in each pair are identical in value to each other, but not necessarily equal to the resistors in the other pair. For example, one pair might consist of two 10k resistors, and the other two might be 20k resistors. Even though the resistance of one pair is double in value of that of the other, the voltage, $\mathrm{V}_{\text {out }}$ at the center nodes of each pair is the same. Can you see why?

In fact, the only way $\mathrm{V}_{\text {out }}$ will change is if one of the resistances changes, and this is where the strain gauge comes in to play. By replacing one of the pairs of resistors in the Wheatstone bridge circuit with the strain gauges that are mounted on the beam, the voltage at their common node will vary according to the strain in the beam. Since one strain gauge is on top, and the other is on the bottom directly beneath it, they will experience equal and opposite strains. Accordingly, their resistance will change by equal and opposite amounts. Also, because of this configuration, the bridge compensates itself for changes in temperature. All of these factors ensure that the circuit

[^1]behaves in a very linear fashion. We will also add a variable resistor, called a trim-pot, between the two fixed resistors, for the purpose of offset correction. That is, we want to make $V_{\text {out }}=0 \mathrm{~V}$ when no force is applied to the beam. (A question to ponder: why is the trim-pot needed if the nominal values of the pair of strain gages and pair of fixed resistors are the same?)


Figure 4 Wheatstone bridge (left) and Wheatstone bridge with offset adjustment (right). The construction of the trimpot (variable resistor) is also shown.
4. Construct the Wheatstone bridge with offset adjustment shown in Figure 4 using the strain gauged cantilever beam, a multi-turn, $1 \mathrm{k} \Omega$ trimpot and two $10 \mathrm{k} \Omega$ resistors on the breadboard. There are 3 leads coming from the strain gauge fixture. One of the three connects to two wires coming from the strain gauges. $\mathrm{V}_{\text {out }}$ will be measured between this lead and the wiper of the trim pot as shown in Figure 4.

Measure the nominal resistance of the strain gauges, both separately and in series, and record the values. Also, measure the value of the other resistance in series, and record these values as well.

Arrange the leads from the strain gage fixture so that the voltage at the node where the two strain gages connect will decrease when a weight is hung on the beam. (To get this right, you will have to remember how a strain gage's resistance responds to strain. When you hang a weight on the beam, the upper gage stretches, and the lower gage shortens.) Once this is accomplished, apply 12 volts to the circuit. Use the voltmeter, and measure $\mathrm{V}_{\text {out }}$. Turn the trimpot screw until $\mathrm{V}_{\text {out }}$ gets as close to zero as you can get it. With $\mathrm{V}_{\text {out }} \approx 0$, the Wheatstone bridge is said to be "balanced." What happens to the voltmeter reading if you press LIGHTLY on the end of the bar?
5. Design and construct a differencing amplifier with a gain of 20 (using the 10 k resistor and inverting amplifier from step 1) as shown in Figure 5. (Just add a 10k and 200k voltage divider to the noninverting terminal as shown in Figure 5.) It is always good practice to try to minimize the length of the input leads to the amplifier and the feedback path. Here, you don't really have a choice, because everything has been pre-wired. If you were going to design this scale as a product, you might want to locate the bridge and amplifier at the base of the cantilever, near the strain gages. (Why?)

Measure the voltage at the output of the op-amp. Adjust the trim pot, and try to get the offset voltage as low as possible.


Figure 5 The electronic scale circuit schematic. The strain gauges are placed in a Wheatstone bridge, and a differencing amplifier amplifies the bridge voltage. A second stage of amplification will be used to increase the signal gain.
6. Connect the output of the differencing amp to the non-inverting terminal of the second amplifier (the non-inverting amplifier with a gain of 50). Now you now have a gain of about $20 \times 50=1000$ from the Wheatstone bridge to the output of the non-inverting amplifier.
Measure the voltage at the output of the non-inverting amplifier. Adjust the trim pot in the Wheatstone bridge, and try to get the offset voltage as low as possible.
Once this is done, press lightly on the bar. What happens to $\mathbf{V}_{\text {out }}$ ? It is important that the output from the second stage of amplification be positive with respect to ground for input to the A/D converter. If the voltage is not positive when you press on the bar, fix the problem before going on.
7. As shown in Figure 6, add a low-pass filter to the output of the second amplifier. Use a 4.7 k resistor and $10 \mu \mathrm{~F}$ capacitor. The idea is to filter out high-frequency noise. What is the cutoff frequency for this filter?


Figure 6 The electronic scale circuit with two stages of amplification and low-pass filter.
8. Determine the overall scale factor of $\mathbf{V}_{\text {out }}$ in Volts/lb by making a series of measurements of known weights. The process of developing the scale factor is called "calibration". Finally, determine the weight of the ins tructor's "unknown" weight.

## Interfacing the Electronic Scale to the Basic Stamp Using an A/D Converter

9. Once you are satisfied with the amplified bridge voltage from Step 8, build the A/D converter circuit shown in Figure 7. An A/D converter is a device that converts an analog voltage into a digital number. The ADC 0831 is an 8 -bit $\mathrm{A} / \mathrm{D}$, which means that it will convert the differential voltage, ( $\mathrm{V}_{\text {in }+}-\mathrm{V}_{\text {in }}$ ), into an 8-bit binary number. The converted voltage will thus be a binary number between 0 and 255 (i.e., $2^{0}$ and $2^{8}$, or 00000000 and 11111111). So what voltage corresponds to which binary number? This correspondence depends on what $\mathrm{V}_{\text {ref }}$ is. When the differential voltage is equal to $\mathrm{V}_{\text {ref }}$, the converted value will be 255 . For example, suppose $\mathrm{V}_{\text {ref }}=5$ V , and the $\mathrm{A} / \mathrm{D}$ is configured as in Figure 7. If $\mathrm{V}_{\mathrm{in}+}=2.51 \mathrm{~V}$, then the digital result will be 128. $\mathrm{V}_{\text {ref }}$ should be between about 1 V and 5 V .
The $\overline{\mathrm{CS}}$ pin is called "chip select". It can be though of as the "chip enable" input. Note the overbar. This means that the chip is enabled (to do A/D conversions) when the $\overline{\mathrm{CS}}$ line is held at logic low. This is called "active low". If the $\overline{\mathrm{CS}}$ line is held at logic high, the chip will not perform any conversions.

The chip is made to do conversions in the following way. Suppose $\overline{\mathrm{CS}}$ is low, an $\mathrm{A} / \mathrm{D}$ conversion is begun when the Clk (clock) line is taken high then low. Then for the next 8 high low transitions of the Clk line, the 8 bits of the conversion will sequentially appear on the DO (data output) line, MSB first. This kind of communication between a microcontroller and a peripheral device such as the A/D chip where the data flows as a stream of bits is called "synchronous serial communication." The word synchronous implies that the stream of bits is handled in lock-step with a clock signal. PBASIC makes it very easy to perform synchronous serial communication using the commands, Shiftin and Shiftout. Since we are acquiring data, we will use the Shiftin command. For more information on how Shiftin works, see the command summary at the end of these instructions or the Basic Stamp Programming Manual.
A PBASIC code fragment that will do a conversion and store the data in a variable called "ADres" is:

```
'Conversion Routine
'Put your name here
'Put the date here
===========================
'Variables and constants
"===========================
CS con 0 'maps the constant CS to pin 0
CLK con 1 'maps the constant CLK to pin 1
AData con 2 'maps the constant AData to pin 2, which will connect to DO of the A/D chip
ADres var byte 'defines ADres as a 1 byte variable, which will hold the A/D result
'===========================
convert: 'label for conversion loop
    low CS 'enables the A/D chip
    shiftin AData, CLK, msbpost, [ADres \9] 'this command handles the conversion
    high CS 'disables the A/D chip
    debug ? ADres 'print out the A/D results
```

```
    pause 1000 'wait for 1 second
goto convert 'do it all again
```

Note that the Shiftin command line gets 9 bits. This is because one clock cycle is needed to start the conversion process, and no valid data is available until the following clock cycle. The bit that gets shifted in on this first clock cycle will just get discarded after the next 8 bits are stored into ADres.

Test this circuit by applying a DC voltage (less than 5 V to the $\mathrm{V}_{\mathrm{in}+} \mathrm{pin}$ of the ADC0831. Make sure that you are able to successfully read and display the voltage applied to the ADC0831 using the Stamp before going on.


Figure 7 The ADC0831 Analog to Digital Converter.
10. Connect the output of the electronic scale to the $\mathrm{V}_{\text {in }+}$ pin of the ADC 0831 . Write a program that will display the weight of an object hanging on the scale.

## Questions*

1. How linear is your relationship of $\mathrm{V}_{\text {out }}$ to the applied weight in lbs?
2. How much did the offset change during your measurements? Why does this happen?
*Other questions are in bold face in the Procedures.
Scope ground clips. If you remember from the first lab, because the circuit uses a common ground, we can attach the ground clips anywhere in the circuit. Actually, we only need to attach one of the ground clips to get a stable trace. Make sure that if you attach both ground clips, you attach them to the same point in the circuit. If you attach them to points at different voltages, you essentially create a shortcircuit to earth ground through your circuit and the 'scope. Such a condition will likely toast your circuit and damage the 'scope, so always think carefully when using the 'scope. For this experiment, it is recommended that you attach one of the ground clips to COM somewhere in your circuit.

## Shiftin

SHIFTIN dpin,cpin,mode,[result $\{\backslash b i t s\}\{$, result $\{\backslash$ bits $\} ..\}$.
Shift data in from a synchronous-serial device.

- Dpin is a variable/constant $(0-15)$ that specifies the I/O pin that will be connected to the synchronous-serial device's data output. This pin's I/O direction will be changed to input and will remain in that state after the instruction is completed.
- Cpin is a variable/constant ( $0-15$ ) that specifies the I/O pin that will be connected to the synchronous-serial device's clock input. This pin's I/O direction will be changed to output.
- Mode is a value ( $0-3$ ) or 4 predefined symbols that tells Shiftin the order in which data bits are to be arranged and the relationship of clock pulses to valid data. Here are the symbols, values, and their meanings:


## Symbol Value Meaning

MSBPRE 0 Data msb-first; sample bits before clock pulse
LSBPRE 1 Data Isb-first; sample bits before clock pulse
MSBPOST 2 Data msb-first; sample bits after clock pulse
LSBPOST 3 Data Isb-first; sample bits after clock pulse
(Msb is most-significant bit; the highest or leftmost bit of a nibble, byte, or word. Lsb is the least-significant bit; the lowest or rightmost bit of a nibble, byte, or word.)

- Result is a bit, nibble, byte, or word variable in which incoming data bits will be stored.
- Bits is an optional entry specifying how many bits $(1-16)$ are to be input by Shiftin. If no bits entry is given, Shiftin defaults to 8 bits.


## Explanation

Shiftin provides an easy method of acquiring data from synchronous-serial devices. Synchronous serial differs from asynchronous serial (like Serin and Serout) in that the timing of data bits is specified in relation-ship to pulses on a clock line. Data bits may be valid after the rising or falling edge of the clock line. This kind of serial protocol is commonly used by controller peripherals like ADCs, DACs, clocks, memory devices, etc. Trade names for synchronous-serial protocols include SPI and Microwire. At their heart, synchronous-serial devices are essentially shift-registers - trains of flip-flops that pass data bits along in a bucket-brigade fashion to a single data-output pin. Another bit is output each time the appropriate edge (rising or falling, depending on the device) appears on the clock line. BS2 application note \#2 explains shift-register operation in detail. A single Shiftin instruction causes the following sequence of events:

- Makes the clock pin (cpin) output low.
- Makes the data pin (dpin) an input.
- Copies the state of the data bit into the msb (lsb- modes) or lsb(msb-modes) either before (-pre modes)or after (-post modes) the clock pulse.
- Pulses the clock pin high for $14 \mu \mathrm{~s}$.
- Shifts the bits of the result left (msb- modes) or right (lsb-modes).
- Repeats the appropriate sequence of getting data bits, pulsing the clock pin, and shifting the result until the specified number of bits is shifted into the variable.

Making Shiftin work with a particular device is a matter of matching the mode and number of bits to that device's protocol.


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