# San José State University

# Computer Science Department

## CS 147, Section 05

## Introduction to Computer Architecture

## Fall, 2014

### Course and Contact Information


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|---|---|
| ***Instructor:*** | Kaushik Patra |
| ***Office Location:*** | DH 282 |
| ***Telephone:*** | (408) 924-5060 |
| ***Email:*** | kaushik.patra@sjsu.edu |
| ***Office Hours:*** | Wednesday 10:30 am – 11:45 am |
| ***Class Days/Time:*** | MW 9:00 am – 10:15 am |
| ***Classroom:*** | MH 422 |
| ***Prerequisites:*** | CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better) |


### Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

#### *Course Topics:*

Hardware Description Languages, Data Representation in Computer Hardware, Computer Arithmetic, Memory Organization, Control Unit Operation and Implementation, Instruction Formats, Pipelining and Vector Processing, Multiprocessing, and RISC Architecture and Principles.

#### *Course Objectives:*

- Review the basic Boolean number representation schemes, digital logic gates, and basic combinatorial and sequential circuit structures.
- Introduction to the basic roles and responsibilities for each of the major hardware components of a computer.
- Review the need to use a memory hierarchy, perform memory management, and to explain to them the various memory management techniques and their tradeoffs.
- Review implementation of the fundamental mathematical operations such as addition, subtraction, multiplication, and division and optimization with Boolean operands.
- Review tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).

- Review non-classical architectures such as parallel processors and pipelined machines which are used to accelerate hardware performance without impacting legacy sequential software programming languages or techniques.
- Introduction to computer-aided design tools and hardware description languages useful to computer architects in performing functional verification and performance measurements of digital systems.
- Review operation of hardware and software working synergistically together.

***Course Goal:***

To examine alternative organizations and architectures associated with the implementation of basic computer hardware functions such as the memory hierarchy and its management, central processing unit (CPU) and arithmetic logic unit (ALU), instruction sets, and RISC.

***Course Learning Outcomes (CLO):***

Upon successful completion of this course, students should be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.
- Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware designs.

***BS in Computer Science Program Outcomes Supported:***

These are the BSCS Program Outcomes supported by this course:

(a) An ability to apply knowledge of computing and mathematics to solve problems.

(b) An ability to analyze a problem, to identify and define the computing requirements appropriate to its solution

(c) An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs

(d) An ability to use current techniques, skills, and tools necessary for computing practice

(e) An ability to apply mathematical foundations, algorithmic principles, and computer science theory in the modeling and design of computer-based systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

**Recommended Texts/Readings –** can be rented or bought used/new from SJSU bookstore

***Textbook :***

COMPUTER ORGANIZATION and DESIGN | Edition: 5
Author: DAVID A. PATTERSON
ISBN:9780124077263
Publication Date:10/10/2013
Publisher:ELSEVIER

***Other Readings :***

COMPUTER ARCHITECTURE | Edition: 5TH 12
Author: HENNESSY
ISBN: 9780123838728
Publication Date: 09/29/2011
Publisher: ELSEVIER

COMPUTER ORGANIZATION and ARCHITECTURE | Edition: 9TH 13
Author: STALLINGS
ISBN: 9780132936330
Publication Date: 03/15/2012
Publisher: PEARSON

VERILOG HDL-W/CD | Edition: 2ND 03
Author: PALNITKAR
ISBN: 9780130449115
Publication Date: 03/10/2003
Publisher: PEARSON

## Course Requirements and Assignments

- Each student is expected to be present, punctual, and prepared at every scheduled class and lab session. It is assumed that the students already have basic knowledge of digital Boolean logic and fundamentals of assembly language machine programming.
- You will be **required** to bring a wireless laptop to all classes.
- Each class session will be divided into lecture (~40 min) and hands-on lab / discussion (~30 min) with 5 min break in between. Attendance is **NOT** optional. Individual participation is also required. There will be no make-ups for missed midterm or assignments, unless any special arrangements is made with the instructor beforehand.
- All student **must complete** the ***Syllabus agreement*** through Canvas quiz by ***Aug 27, 2014 12:00 noon***. Any one **failed** to do so will be **dropped** from the class.
- There will be **3 home works** and **3 individual projects,** one **midterm** and **final exam**. All home works and projects should be submitted through Canvas. **No scanned copy** of handwritten solution is allowed. Allowed document types are PDF / ODT / DOC.

Project report should contain the following.

- Introduction containing objective.
- Requirement.
- Design and Implementation.
- Testing
- Conclusion
- Make sure to
    1. Include clear diagrams for requirement and design.
    2. Include code snippet to explain implementation.
    3. Include screen shots of testing waveforms and results.
    4. Upload HDL source code and test program as zip archive.

Project reports are encouraged to be submitted in IEEE format.
[ http://www.ieee.org/conferences_events/conferences/publishing/templates.html ]

***10% of the obtained marks will be awarded as extra points in project evaluation if report submitted in proper IEEE format.***

## Grading Policy

1. Homework carries **30%** towards final score. Average of 3 score from homework will be contributed.
2. Project carries **30%** towards final score. Average of 3 score from projects will be contributed.
3. Midterm carries **20%** towards final score.
4. Final carries **20%** towards final score.

Submission is allowed till **11:59 pm on due date**. Zero delay tolerance for the submission, i.e. NO late submission is permitted, unless you make special arrangements with your instructor beforehand.

You will receive a numeric score for the midterm, the final, each of the total homework, and each project submission. Letter grade, which is your class grade, will be obtained by adding the numeric scores and weighing with the percentages given below. Fraction in percentage will be converted into nearest integer value ('>= 0.5' will be moved to next integer number, '< 0.5' will be moved to previous integer number).

| | | |
|---|---|---|
| A+ = 100-97% | A = 96-93% | A- = 92-90% |
| B+ = 89-87% | B = 86-83% | B- = 82-80% |
| C+ = 79-77% | C = 76-73% | C- = 72-70% |
| D+ = 69-67% | D = 66-63% | D- = 62-60% |
| F = 59-0% Failure | | |

*"Students are strongly encouraged to take courses to satisfy GE Areas R, S, and V from departments other than their major department. Passage of the Writing Skills Test (WST) or ENGL/LLD 100A with a C or better (C- not accepted), and completion of Core General Education are prerequisite to all SJSU Studies courses. Completion of, or co-registration in, 100W is strongly recommended. A minimum aggregate GPA of 2.0 in GE Areas R, S, & V shall be required of all students." See University Policy S14-5 at http://www.sjsu.edu/senate/docs/S14-5.pdf."*

## Classroom Protocol

1. **You must come to class on time!** Students entering the classroom late disrupt the lecture and / or the students already in class who may be engaged in lab or discussion. Late students will not be accepted in class.

2. If you miss a lecture you are still responsible for any material discussed or assignments given. A large portion of each class will be used for hands-on lab / discussion. All students are expected to participate in class activities. Students who are often absent will find themselves at a disadvantage during the tests.

3. No audio / video recording or photography in the classroom without prior permission of instructor.

4. No personal discussion or cell phone activity during class time. Please set the cell phone on **silent/vibrate** mode.

5. All e-mail communication to the instructor must have the *subject* line start with **[CS-147, 05]**

6. Email to be sent to the instructor's SJSU email ID (kaushik.patra@sjsu.edu) only.

## University Policies

***Dropping and Adding:***

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic year calendars document on the Academic Calendars webpage at http://www.sjsu.edu/provost/services/academic_calendars/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/**.** Students should be aware of the current deadlines and penalties for dropping classes. Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

***Consent for Recording of Class and Public Sharing of Instructor Material :***

University Policy S12-7, http://www.sjsu.edu/senate/docs/S12-7.pdf, requires students to obtain instructor's permission to record the course :

- "Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor's permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material."
- "Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent."

***Academic integrity :***

Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The University Academic Integrity Policy S07-2 at http://www.sjsu.edu/senate/docs/S07-2.pdf requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sjsu.edu/studentconduct/.

***Campus Policy in Compliance with the American Disabilities Act :***

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 at http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf requires that students with disabilities requesting accommodations must register with the Accessible Education Center (AEC) at http://www.sjsu.edu/aec to establish a record of their disability.

***Accommodation to Students' Religious Holidays :***

San José State University shall provide accommodation on any graded class work or activities for students wishing to observe religious holidays when such observances require students to be absent from class. It is the responsibility of the student to inform the instructor, in writing, about such holidays before the add deadline at the start of each semester. If such holidays occur before the add deadline, the student must notify the instructor, in writing, at least three days before the date that he/she will be absent. It is the responsibility of the instructor to make every reasonable effort to honor the student request without penalty, and of the student to make up the work missed. See University Policy S14-7 at http://www.sjsu.edu/senate/docs/S14-7.pdf.

**Course Schedule (tentative) –** *subject to change by instructor with due notice.*

| Date | Lecture | Lab | Notes |
|---|---|---|---|
| 08/25/14 | Intro CS147 | | |
| 08/27/14 | Introduction to computer<br>Basic Instruction Set<br>ALU | Tool Setup | **Turn-in deadline for Syllabus agreement by 12:00 noon.**<br>**Need to send pre-req proof by 8/29** |
| 09/01/14 | Labor Day (Campus Closed) | | |
| 09/03/14 | Memory Controller<br>Von Neuman Arch<br>System software | Simulation<br>Project<br>Example | Add code will be supplied by 09/02/14 midnight.<br>Project-I will be up. |
| 09/08/14 | Digital Synthesis<br>Number Representation | Hierarchical Models | Homework 1 will be up. |
| 09/10/14 | Boolean Algebra Review | Data Flow Modeling | Project II will be up. |
| 09/15/14 | Boolean Algebra Review | Data Flow Modeling | **Report due for Project I** |
| 09/17/14 | Comb/Seq logic | Data Flow Modeling | |
| 09/22/14 | Comb/Seq logic<br>Addition / Subtraction | Data Flow Modeling | Project I evaluation will be returned. |
| 09/24/14 | Multiplication | Behavioral Modeling | |
| 09/29/14 | Division | Behavioral Modeling | |
| 10/01/14 | Shifter / Mux / Decoder | Behavioral Modeling | |
| 10/06/14 | Design Flow<br>Instruction Set Architecture | Behavioral Modeling | **Homework 1 is due. Solution will be posted by 10/07 midnight.** Homework 2 is up. |
| 10/08/14 | RISC / CISC<br>Midterm review | Behavioral Modeling | |
| 10/13/14 | **Midterm Exam** | | |
| 10/15/14 | Pipeline architecture | Project II | Project III will be up |
| 10/20/14 | Pipeline architecture | Project II | Homework 1 evaluation will be returned. |
| 10/22/14 | Multicore architecture | Gate Level Modeling | **Report due for Project II** |
| 10/27/14 | Multicore architecture | Gate Level Modeling | |
| 10/29/14 | Vector processing | Gate Level Modeling | |
| 11/03/14 | Hardware threading | Gate Level Modeling | |
| 11/05/14 | Memory Hierarchy<br>Internal Memory | Advanced HDL topic | Project II evaluation will be returned.<br>Homework 3 is up. |
| 11/10/14 | Internal Memory | Advanced HDL topic | **Homework 2 is due. Solution will be posted by 11/11 midnight.** |
| 11/12/14 | Internal Memory | Advanced HDL topic | |
| 11/17/14 | External Memory | Advanced HDL topic | |
| 11/19/14 | External Memory | Project III | Home work 2 will be returned |
| 11/24/14 | Input/Output | Project III | **Homework 3 is due. Solution will be posted by 11/25 midnight.** |
| 11/26/14 | Input/Output | Project III | |
| 12/01/14 | Interconnects | Advanced HDL topic | **Report due for Project III** |
| 12/03/14 | Interconnects | Advanced HDL topic | Home work 3 will be returned |
| 12/08/14 | OS Support | Advanced HDL topic | |
| 12/10/14 | OS Support<br>Final Exam Review | Advanced HDL topic | Project III evaluation will be returned. |
| 12/16/14 | **Final Exam @ 7:15 AM (MH422)** | | |