RF OUTPUT WINDOW DESGIN FOR A HELIX TRAVELING WAVE TUBE

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Abstract: An output circuit of a helix traveling wave tube was modeled in High Frequency Structure Simulation (HFSS) 3D software. The challenge was to first determine how to model the circuit in HFSS and later match the model results to real measurements made with hardware. Upon the agreement of the model and hardware results a design change was attempted to make the circuit have a better VSWR than 1.5:1 in the frequency range of 12-18GHz. After making few changes in the geometry the circuit was able to give a VSWR less than 1.5:1.

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I. **INTRODUCTION**

Traveling Wave Tubes are high frequency wide band amplifiers that are used in nearly all communication systems. They operating frequency can range from 1-100GHz and can put out power from Watts-Megawatts. Microwave tubes are the answer to the failure of operation of solid state devices at high frequency. In solid state devices as the wavelength approaches the element size, the lumped elements behave in an unpredictable manner. As a result of this fact Traveling Wave tubes dominate the high frequency spectrum and find use in most military applications.

II. **BACKGROUND AND THEORY**

A TWT consists of an electron gun, slow wave circuit and a collector as shown in Figure 1

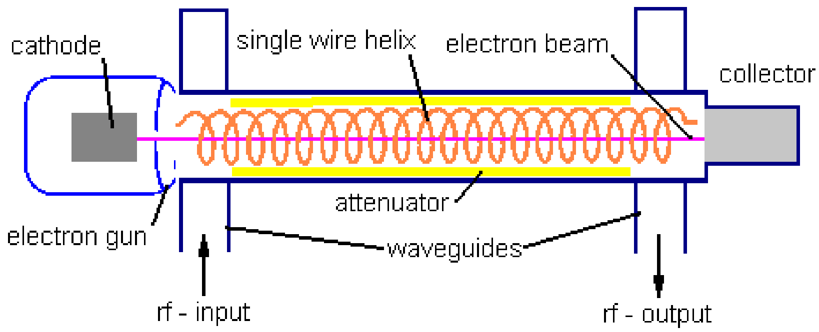


Figure 1: *Basic Schematic of a TWT Setup*

The electron gun is responsible for generating the beam needed for amplification. The slow wave structure makes the interaction between RF and electron beam possible. The collector is on the opposite end of the gun and consumes the remainder of the beam from the interaction. The RF wave amplification process occurs by extracting energy from electron beam that generated by the cathode. An electron beam is generated in the same manner as most conventional televisions. That is why all the TWT have to maintain a vacuum level. A cathode is heated up to its proper temperature so it can start emitting electrons. The beam then enters the slow wave structure and it held together by the magnetic field of magnets. The traveling speed of electron is a lot slower than the RF wave and that is why a slow wave structure is needed. A slow wave structure can be defined as any geometry that can slow down the RF wave to match the speed of the beam. In our case the slow wave structure is the helix. The output circuit window as seen in Figure 2 which is the main concern of this project, is responsible to transferring all the power from the slow wave structure to the output connector.

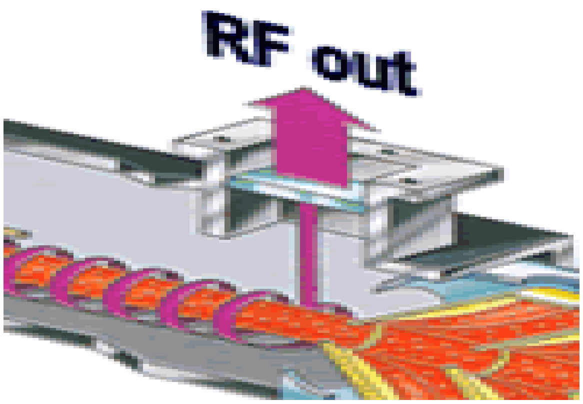


Figure 2: *Basic View of The Output Window*

This is one of the most critical components of a TWT. An output circuit window is responsible for transferring the power to the output connector and also provides a vacuum seal at the same time. Improving the output circuit VSWR performance means making the TWT more efficient in power handling.

The software chosen to model this circuit is HFSS. This software solves for Electric field in given structures and can give VSWR, RL, S-parameter values and other related quantities on any modeled geometry. 3D capabilities of HFSS allow the user to draw real life structures and make changes as desired. Once the geometry is modeled in HFSS it is very simple to go and make a change in the model design. This process is more efficient than building and testing one circuit at a time.

III. **PROCESS**

The output circuit consists of helix, coaxial output window and coaxial connector as shown in Figure 3

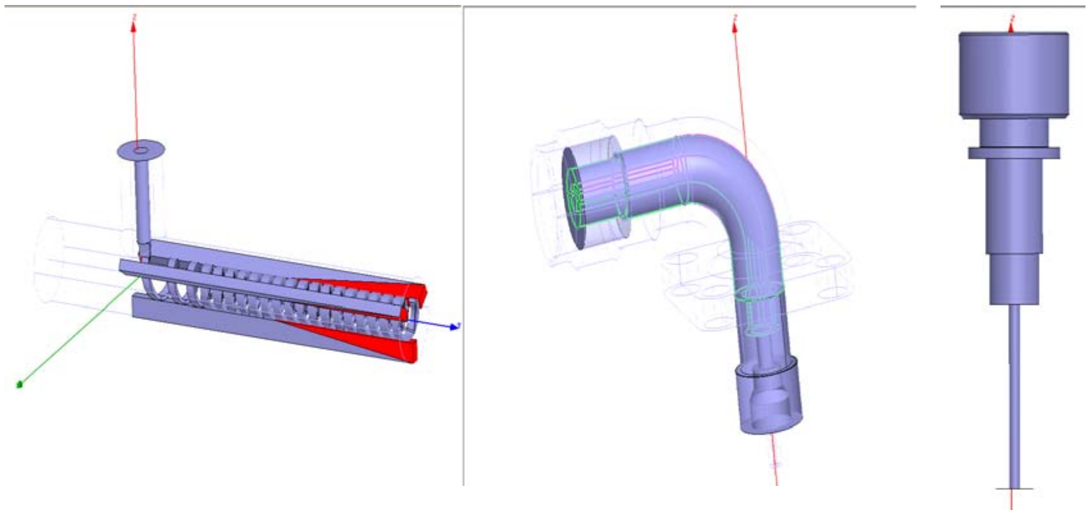


Figure 3: *Helix Circuit, Coaxial Connector & Output Window*

The project kick-off faced two challenges simultaneously. A TWT had never been modeled in HFSS and capabilities of HFSS version 9.0 were unknown. The only known information was that HFSS version 8.5 could not handle more than six turns of a helix. The original real hardware circuit has 74 turns. The possibility of having that many turns modeled is impossible due to memory limitations in the computer memory. The projected methodology was to model the coaxial output window and make a change. However since output window is part of a bigger circuit, other pieces like helix and coaxial connector also had to be solved for VSWR and incorporated into the output window model. The project began by having constructed initial model of the circuit by having nine turns of the helix. The initial intention was to solve for the match for the helix circuit and then assigned VSWR properties to the bottom section of the output window as shown in Figure 4

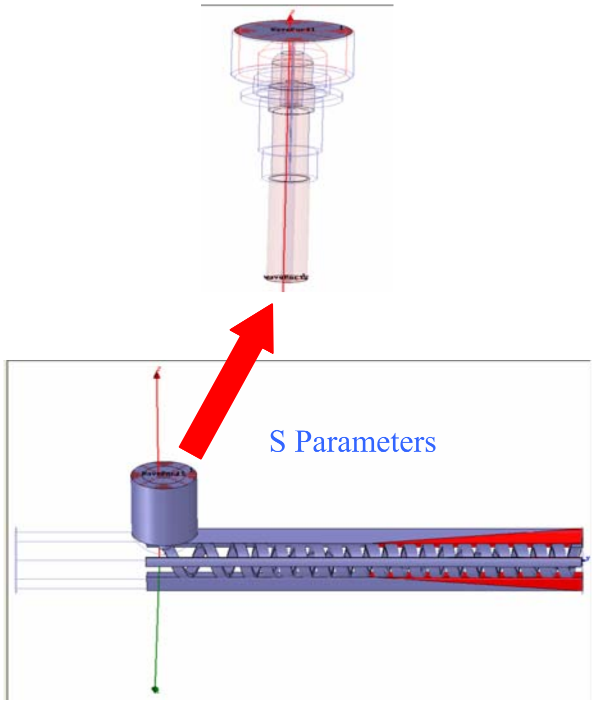


Figure 4: *Ideology of Assigning Wave Ports with S Parameters.*

However it was realized that excitation ports in HFSS could not be assigned and VSWR characteristics and it was a dead end. This meant that the project could not be solved in pieces. At this point a new version of HFSS called 9.2.1 came out that was capable of handling more memory. It was realized that this version could solve for 19 turns. The reason for having 19 turns in the model was to make sure to have enough turns to approximate to 74 turns of a real hardware circuit. The coaxial output window was added on top of the helix model and solved successfully as shown in this figure.

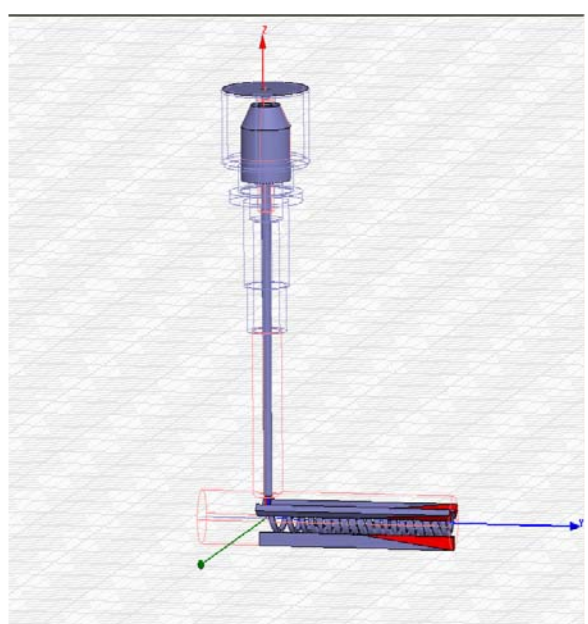
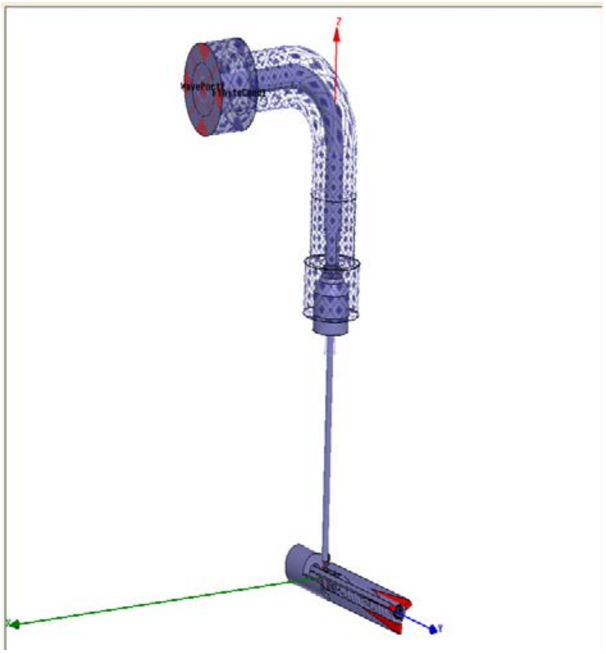


Figure 5: *Output Window and Helix as one piece*



At this stage, the coaxial connector was the only piece missing from the model. At last it was also added to see if HFSS would be capable to solving it as shown in this figure 6. After 75 model iteration, we had a complete model of the output circuit that was solved and was officially the biggest ever helix circuit to solve in HFSS.

Figure 6: *The Complete Output Circuit*

IV. **MODELING DECISIONS**

Many critical modeling decisions had to be made in order to match the HFSS model to approximate to the hardware circuit. The first challenge was to determine how to introduce the attenuation in the circuit to approximate it as a one port device. Chopping off the circuit in pieces attenuates the original TWT circuit. We started out by introducing the loss away from the helix (shown in Figure 7) and realized the attenuation was not sufficient.

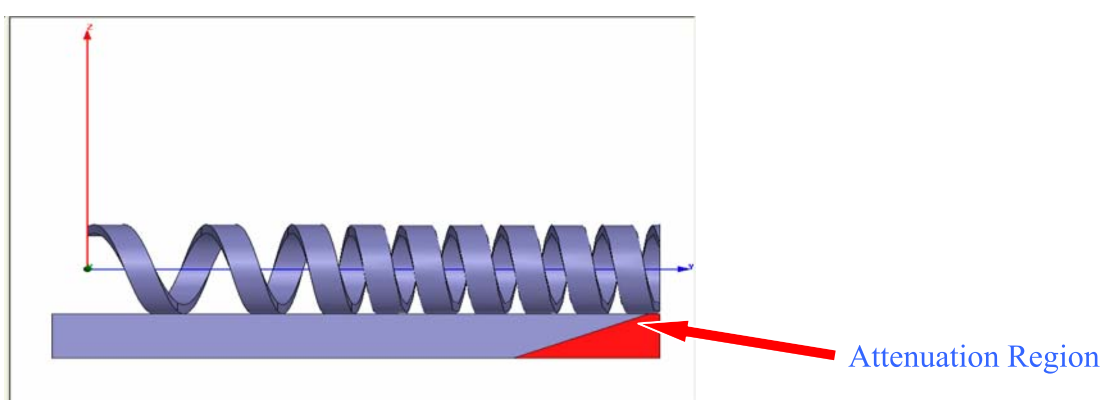


Figure 7: *Attenuation Away From the Helix*

We determined this by looking at the E-field across the circuit. Visibility of any magnitude of E-field in the attenuation region meant reflections. The loss pattern was settled by introducing the loss closer to helix as shown in Figure 8

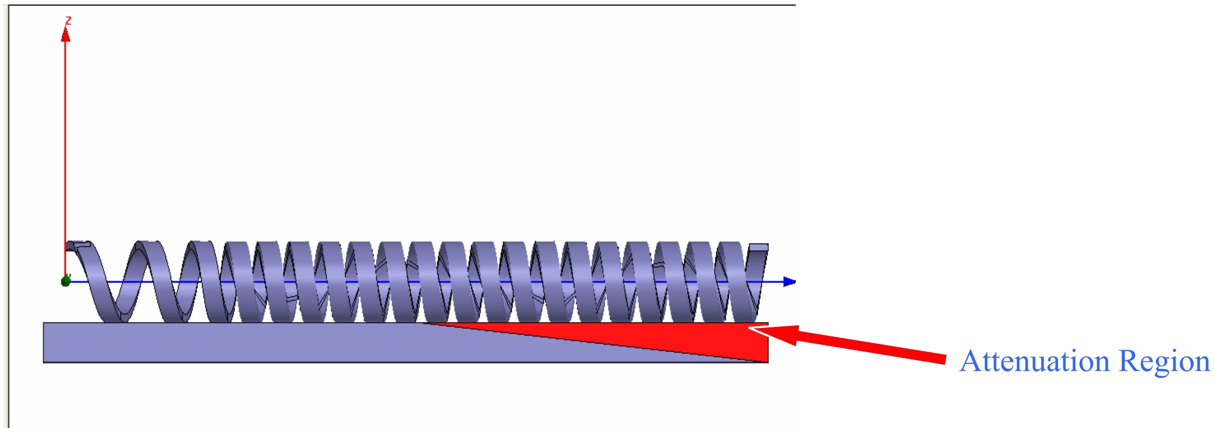


Figure 8: *Attenuation Close To the Helix*

The E-field in this case died out down to almost zero indicating that the wave has been attenuated properly.

Constructing the tape (Figure 9) was the next big issue. It was realized that the tape geometry had a huge impact on the match. The initial tape geometry was straight piece that connected the center conductor of the window and the helix. The tape in the real circuit is swept from one side to the other.

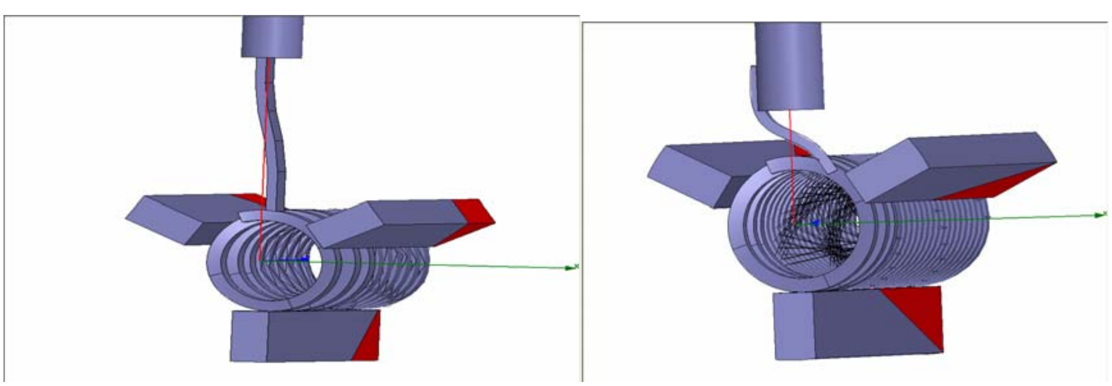


Figure 9: *Straight and Circular Tape Geometries*

This was eventually accomplished after many trials of construction in the program. Totals of five-tape geometries were tried and the one that gave the best VSWR was chosen as a standard to represent the hardware geometry. Last decision came about the inclusion of matching fingers shown in Figure 10. In hardware circuit matching fingers are used to tune the impedance by moving their relative position to the helix. Our test circuit had matching fingers in them and it was discovered that they also helped the VSWR significantly. Matching fingers were added at the very end once it was discovered that rest of the circuit could be solved.

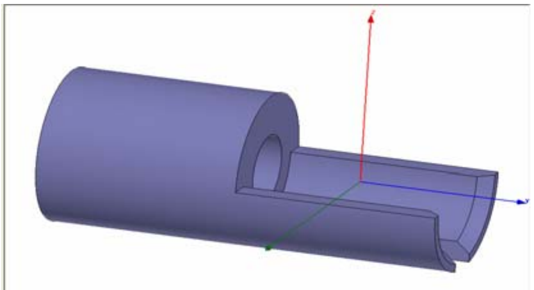
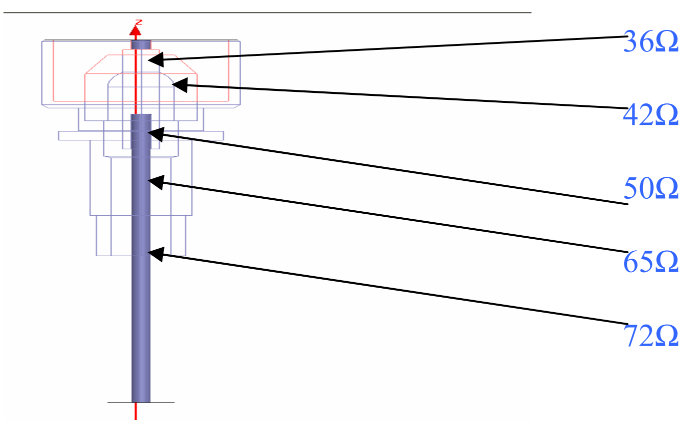


Figure 10: *Matching Fingers*

V. **DISCOVERIES**

The hardware circuit was analyzed in detail in order to be modeled. Each component dimension was examined to be drawn into the model. Many errors were discovered during this process. The main error came from the impedance steps of the output window. The very top of the window is supposed to be matched to a 50ohm load. Our calculations discovered that this was not the case (figure 11) and were confirmed by Time Domain Reflectometry (TDR), which was the next discovery



Main Formula

$$Zo = \frac{138\log(D/d)}{Er^{0.5}}$$

Figure 11: *Impedance Steps Calculations*

TDR is an option in HFSS that was explored for this first time using out model. It yields a time versus in circuit impedance. TDR confirmed that the very top of the output window was not matched to 50 ohms by illustrating it through a plot shown in Figure 12.

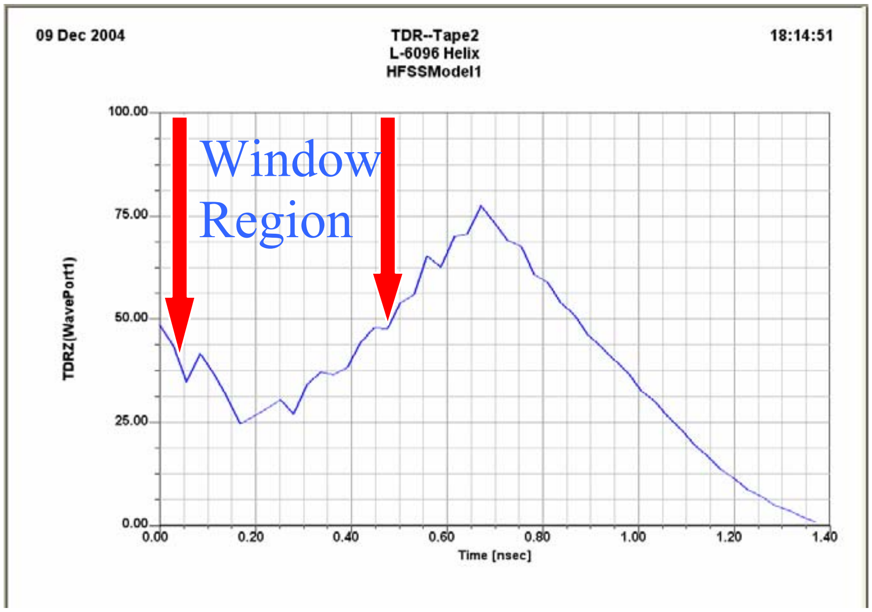


Figure 12: *TDR Plot Generated with HFSS*

It also helped with understanding the behavior of helix in circuit impedance. Helix impedance is a quantity that can easily be calculated but it's in circuit value was still a mystery. TDR helps us see how the helix impedance can change by adding of removing components around it.

Sharp edges (figure 13) are disliked by HFSS and can cause a solution to fail. Every time a small sharp edge is created HFSS has to refine its mesh size small enough to approximate the surface. This in return yields a bigger problem for the

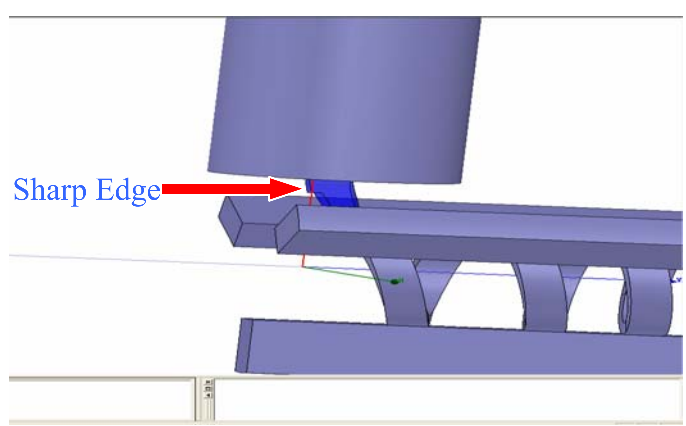
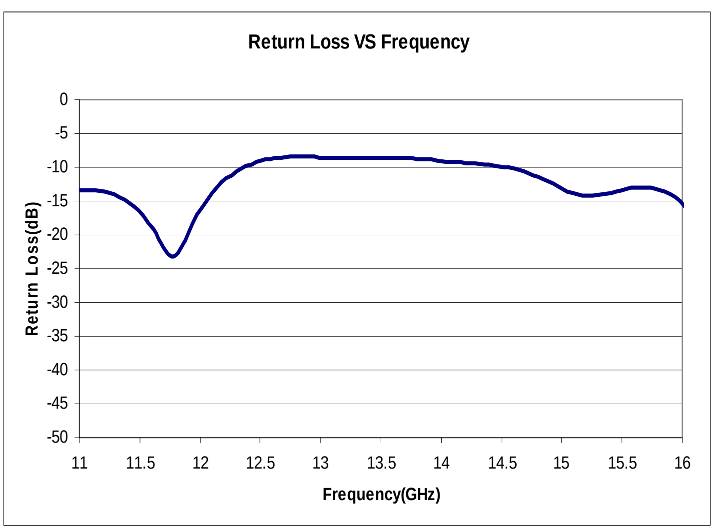


Figure 13: *Sharp Edge Instance causing program to fail*

program to solve and can easily reach the memory limit since our model was initially quite large. This was discovered while drawing the tape in HFSS. Tape left off very tiny edges that very often caused the program to run out of memory.

VI. **RESULTS**

A match with in the desired specifications was achieved by altering the tape geometry and correcting the impedance by making the outer conductor wider in the coax window to yield 50 ohms on the very top. It was learned that tape contributes to a lot of internal reflections in the circuit. The new tape is a longer piece that will allow a smoother transition from the coax to the helix. These changes were implemented in the model and showed a promising change. Now they will be tried out in the real hardware to see if their discovery can be utilized to optimize the efficiency of the circuit. Figure 14 shows the original return loss (RL) graph generated by HFSS and the network analyzer.



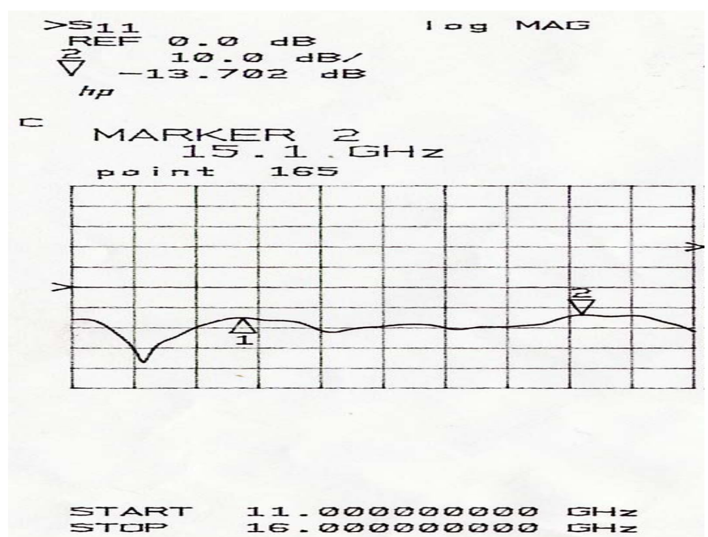


Figure 14: *RL vs. Frequency graphs generated by HFSS and the network analyzer*

It can be observed that the general shape is the same and the magnitude of the RL is a lot better in the improved match (Figure 15) and we have a much better response in the desired high frequency range.

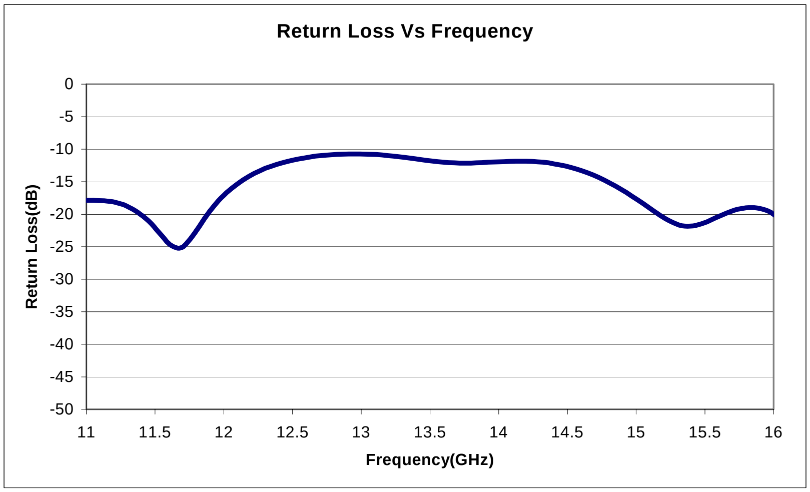


Figure 15: *RL vs. Frequency Graph with the New Tape Geometry*

VII. **CONCLUSION**

This project explored many areas from research, hardware and design. There many questions answered about the helix properties that will help in the future design. The process used in this project indicates that a whole TWT output circuit can be modeled and solved successfully. This procedure will also set a future trend of modeling by avoiding a lot of the modeling attempts done here.