San José State University
Charles W. Davidson College of Engineering
DEPARTMENT OF ELECTRICAL ENGINEERING
EE271-01 - Advanced Digital System Design and Synthesis (Spring 2016)

Instructor: Prof. Thuy T. Le
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Email: Thuy.Le@sjsu.edu
Office Hours: Monday & Wednesday, 16:00 – 18:00
Class Days/Time: Monday & Wednesday, 18:00 – 19:15
Classroom: Engineering Building, room 345
Prerequisites: Graduate standing. Experiences in digital/logic design. Background in integrated circuit design is helpful. Must have self-motivations in self-learning EDA tools and Verilog HDL

Faculty Web Page and MYSJSU Messaging
Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on the Canvas learning management system course website at http://sjsu.instructure.com. You are responsible for regularly checking with your official email address (email address stored on your MySJSU account) to learn of any updates from the course instructor. Additional information can be found on my faculty profile web page at www.sjsu.edu/people/thuy.le/

Course Description
This course covers topics in the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of logic and system design, synthesis, and optimization for area, speed and power consumption. The course enables students to apply their knowledge for the design of advanced digital hardware systems with corresponding EDA tools. Verilog HDL will be used for simulation and synthesis of the homework assignments and final design project.

Course Learning Outcomes
Upon successful completion of this course, students will be able to:

CLO 1. Design and manually optimize complex combinational and sequential digital circuits
CLO 2. Model combinational and sequential digital circuits by Verilog HDL
CLO 3. Design and model digital circuits with Verilog HDL at the algorithm (behavioral) and data flow (RTL) levels as well as with behavioral and structural languages.
CLO 4. Develop testbenches to verify the design by simulation and analysis
CLO 5. Perform functional and timing verifications of digital circuits
CLO 6. Perform static and dynamic timing analysis with false paths and hazards
CLO 7. Synthesis combinational and sequential circuits with trade-offs in timing, area, and power
CLO 8. Understand the relationships between timing performance, parallelizing and pipelining
CLO 9. Understand fundamental principles of analyzing power distribution and optimizing power consumption in digital circuits

Required Texts, Reading Materials, UNIX Accounts and EDA Tools

Textbooks
- EE271 Lecture Notes by Thuy T. Le (available on class canvas)
  Each chapter will be posted on Canvas two weeks before the start of the lecture and will be deleted once the lecture discussion started in class. Requests for reposting lecture notes will NOT be considered.

Additional Readings (optional)
- Any “Verilog Language” books/notes. Below are few on-line documents:
  http://www.doulos.com/knowhow/verilog_designers_guide/
  http://www.sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html
  http://www.nandland.com

UNIX Accounts on Cadence Laboratory
- Rooms E289 and E291 are Cadence laboratories installed with Cadence and Synopsys software tools. Each registered SJSU student should automatically have a UNIX account. If you do not know your login name and password (or having problems with the account), you can find out at https://unix.engr.sjsu.edu/wiki/doku.php
- For Unix tutorial materials and other documents related to Cadence laboratory, please consult Prof. Parent’s website at www.sjsu.edu/people/david.parent/

EDA Tools
- Synopsys Verilog Compiler Simulator (VCS) (required): Available on SJSU Cadence Lab
- Synopsys Design Compiler (required): Available on SJSU Cadence Lab
- Cadence NC-Verilog Simulator (optional): Available on SJSU Cadence Lab
- Any other Verilog simulators (such as ModelSim PE (optional), which can be downloaded at http://www.mentor.com/company/higher_ed/modelsim-student-edition)

Course Requirements and Assignments

Lectures
The course will follow the selected subjects as listed on the course description. Additional theory and examples will be given and discussed in class as much as time permits. Please note that lecture materials are NOT solely based on the required text and so students are responsible for following up the lecture in order to prepare themselves for the exams.
- Students are responsible for the reading the text, handouts, lecture presentations, etc.
– Students are responsible for following up and keeping track of the in-class lecture materials.
– Students are responsible for finding and reading additional books, papers, examples, etc. in order to gain more understanding of the materials discussed in the lectures.
– Students are responsible for self-learning and using of EDA tools for assigned homework problems, lab exercises, projects, and for lecture discussions.

Exams and Final Design Project

There will be one midterm exam, a comprehensive final exam, and an individual final design project with report. The exam and project due dates are listed on the course schedule section of this syllabus. Since make-up exams will NOT be allowed, please make sure that you are able to attend all exams at the indicated scheduled dates and times (from the beginning of the semester) in order to register for the course.

– **Please do NOT ask for sample exam**
  – All exams are closed-book exams.
    · One sheet (double-side) of hand-written notes is allowed for the midterm exam and two sheets of hand-written notes are allowed for the final exam.
    · Summary (printed) of Verilog keywords is allowed and is available on class Canvas. Please download this summary and have it with you during the exam.
    · Some complex information will be provided if needed.
    · Only basic calculators are allowed.
    · **Exam questions will NOT be interpreted during the exam.**
  – There will be no make-up exams (in very special circumstances, written excuse and official proofs are required for making-up exams).
  – Exam solutions will be discussed in class after the exam dates. Written solutions will NOT be distributed.

Homework Assignments and Lab Exercises

Seven homework assignments and/or lab exercises will be given with due dates as shown on the syllabus. Homework must be submitted in class and solutions will be available after the due date.

– Do NOT submit HW via email. Submit HWs in class as hard-copies (paper) only
– Late submission will NOT be accepted (absolutely!).
– There is no make-up homework/lab
To get credit for your homework/lab assignments, submissions must be neat, clean, and must be done professionally and seriously. Your official name (not nickname), course #, and homework # must be visibly shown on each assignment.

Grading Policy

The overall course grades (letter-grades) will be assigned based on a defined grading standard as shown below. The weights of the whole course work assignments are:

- Homework assignments and lab exercises: 10%
- A closed-book midterm exam: 25%
- A closed-book comprehensive final exam: 45%
- An individual final design project and project report: 20%

And the overall course grade (letter-grade) will be assigned based on the distribution below:

- 100% to 81%: Distributed for A+, A, and A-
Classroom Protocol

EE271 students understand that professional attitude is necessary to maintain a comfortable academic environment in the classroom. For examples:

- Students will put their cell phones in quiet/vibration mode during the lecture.
- Students understand that drinking water, juices, etc. during the lecture is acceptable but NOT eating.
- Students will not skip the lecture and then ask the instructor to summarize the lecture later on. Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.
- Students will come to the class on time and leave the class at the end of the lecture.
- Students will consult the course syllabus for class policies and requirements before requesting the instructor for any special considerations and/or exceptions.
- To minimize possible tension during the exams, students are requested to follow the exam rules closely.
- Students will work on the project and report by their own and will not share the work with other students.
- Students understand that long-term learning is their responsibility and will always keep it up.

If you need explanations on lecture materials, projects, homework assignments, exams, etc.... please see me in-person during my office hours. Do NOT email me for these matters. If you must send me an email, please clearly specify your full-name, course, section, etc. I will not respond to email that I do not know the author or emails that have no manners.

University Policies

General Expectations, Rights and Responsibilities of the Student

As members of the academic community, students accept both the rights and responsibilities incumbent upon all members of the institution. Students are encouraged to familiarize themselves with SJSU’s policies and practices pertaining to the procedures to follow if and when questions or concerns about a class arises. To learn important campus information, view University Policy S90–5 at http://www.sjsu.edu/senate/docs/S90-5.pdf and SJSU current semester’s Policies and Procedures, at http://info.sjsu.edu/static/catalog/policies.html. In general, it is recommended that students begin by seeking clarification or discussing concerns with their instructor. If such conversation is not possible, or if it does not address the issue, it is recommended that the student contact the Department Chair as the next step.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Add/drop deadlines can be found on the current academic year calendars document on the Academic Calendars webpage at
http://www.sjsu.edu/provost/services/academic_calendars/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/. Students should be aware of the current deadlines and penalties for dropping classes. Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

Consent for Recording of Class and Public Sharing of Instructor Material

University Policy S12-7, http://www.sjsu.edu/senate/docs/S12-7.pdf, requires students to obtain instructor’s permission to record the course and the following items to be included in the syllabus:

- “Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor’s permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material.”
  - It is suggested that the greensheet include the instructor’s process for granting permission, whether in writing or orally and whether for the whole semester or on a class by class basis.
  - In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.
- “Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent.”

Academic integrity

Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The University Academic Integrity Policy S07-2 at http://www.sjsu.edu/senate/docs/S07-2.pdf requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sjsu.edu/studentconduct/.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 at http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf requires that students with disabilities requesting accommodations must register with the Accessible Education Center (AEC) at http://www.sjsu.edu/aec to establish a record of their disability.

Student Technology Resources

Computer labs for student use are available in the Academic Success Center at http://www.sjsu.edu/at/asc/ located on the 1st floor of Clark Hall and in the Associated Students Lab on the 2nd floor of the Student Union. Additional computer labs may be available in your department/college. Computers are also available in the Martin Luther King Library. A wide
variety of audio-visual equipment is available for student checkout from Media Services located in IRC 112. These items include DV and HD digital camcorders; digital still cameras; video, slide and overhead projectors; DVD, CD, and audiotape players; sound systems, wireless microphones, projection screens and monitors.

**SJSU Writing Center**

The SJSU Writing Center is located in Clark Hall, Suite 126. All Writing Specialists have gone through a rigorous hiring process, and they are well trained to assist all students at all levels within all disciplines to become better writers. In addition to one-on-one tutoring services, the Writing Center also offers workshops every semester on a variety of writing topics. To make an appointment or to refer to the numerous online resources offered through the Writing Center, visit the [Writing Center website](http://www.sjsu.edu/writingcenter) at http://www.sjsu.edu/writingcenter. For additional resources and updated information, follow the Writing Center on Twitter and become a fan of the SJSU Writing Center on Facebook. (Note: You need to have a QR Reader to scan this code.)

**SJSU Counseling and Psychological Services**

The SJSU Counseling and Psychological Services is located on the corner of 7th Street and San Carlos in the new Student Wellness Center, Room 300B. Professional psychologists, social workers, and counselors are available to provide confidential consultations on issues of student mental health, campus climate or psychological and academic issues on an individual, couple, or group basis. To schedule an appointment or learn more information, visit [Counseling and Psychological Services website](http://www.sjsu.edu/counseling) at http://www.sjsu.edu/counseling.

**EE Honor Code - Honesty and Respect for Others and Public Property**

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Copy project information from others
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor.”

**Measures Dealing with Occurrences of Cheating**
Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.

A student’s second offense in any course will result in a Department recommendation of suspension from the University.

Course Schedule (tentative)

Schedule is subject to change with fair notice by email and class announcement

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<td>Lecture Note #4 (continue)</td>
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<tr>
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<tr>
<td></td>
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<td>Lecture Note #7 (continue)</td>
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<td></td>
<td>05/18/2016</td>
<td>Final Examination: Wednesday, 17:15 - 19:30</td>
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