San José State University

Computer Science Department

CS 147, Section 01

Introduction to Computer System

Spring, 2017

Course and Contact Information

Instructor:	Kaushik Patra
Office Location:	DH 282
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Email:	kaushik.patra@sjsu.edu
Office Hours:	Tue/Thu 4:30 pm – 5:45 pm
Class Days/Time:	TTh 6:00 pm – 7:15 pm (Sec01)
Classroom:	DH 351
Prerequisites:	CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)

Course Format

This course uses hybrid style. In general students are expected to have computer systems with internet connection. A tool 'ModelSim' will be used to study hardware operation concepts. The materials are uploaded in Canvas prior to class. Students are encouraged to review the lecture note before coming to class. During class hour it is expected that students bring their laptop with internet connection to download some simulation material to work on during class hour if needed. All the homework and assignments are to be uploaded in Canvas.

Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Topics:

Hardware Description Languages, Data Representation in Computer Hardware, Computer Arithmetic, Memory Organization, Control Unit Operation and Implementation, Instruction Formats, Pipelining and Vector Processing, Multiprocessing, and RISC Architecture and Principles.

Course Objectives:

- Review the basic Boolean number representation schemes, digital logic gates, and basic combinatorial and sequential circuit structures.
- Introduction to the basic roles and responsibilities for each of the major hardware components of a computer.
- Review the need to use a memory hierarchy, perform memory management, and to explain to them the various memory management techniques and their tradeoffs.
- Review implementation of the fundamental mathematical operations such as addition, subtraction, multiplication, and division and optimization with Boolean operands.
- Review tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).
- Review non-classical architectures such as parallel processors and pipelined machines which are used to accelerate hardware performance without impacting legacy sequential software programming languages or techniques.
- Introduction to computer-aided design tools and hardware description languages useful to computer architects in performing functional verification and performance measurements of digital systems.
- Review operation of hardware and software working synergistically together.

Learning Outcomes and Course Goals

Course Goal:

To examine alternative organizations and architectures associated with the implementation of basic computer hardware functions such as the memory hierarchy and its management, central processing unit (CPU) and arithmetic logic unit (ALU), instruction sets, and RISC.

Course Learning Outcomes (CLO):

Upon successful completion of this course, students should be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.
- Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware designs

BS in Computer Science Program Outcomes Supported:

These are the BSCS Program Outcomes supported by this course:

a) An ability to apply knowledge of computing and mathematics to solve problems.

b) An ability to analyze a problem, to identify and define the computing requirements appropriate to its solution

c) An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs

d) An ability to use current techniques, skills, and tools necessary for computing practice

e) An ability to apply mathematical foundations, algorithmic principles, and computer science theory in the modeling and design of computer-based systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

Required Texts/Readings – can be rented or bought used/new from SJSU bookstore

Textbook

COMPUTER ORGANIZATION and DESIGN | Edition: 5
Author: DAVID A. PATTERSON
ISBN:9780124077263
Publication Date:10/10/2013
Publisher:ELSEVIER

Other Readings

COMPUTER ARCHITECTURE | Edition: 5TH 12
Author: HENNESSY
ISBN: 9780123838728
Publication Date: 09/29/2011
Publisher: ELSEVIER

LOGIC & COMPUTER DESIGN FUNDAMENTALS
Author: MANO & KIME
ISBN: 9780131989269
Publication Date: 06/15/2007
Publisher: PEARSON

COMPUTER ORGANIZATION and ARCHITECTURE | Edition: 9TH 13
Author: STALLINGS
ISBN: 9780132936330
Publication Date: 03/15/2012
Publisher: PEARSON

VERILOG HDL-W/CD | Edition: 2ND 03
Author: PALNITKAR
ISBN: 9780130449115
Publication Date: 03/10/2003
Publisher: PEARSON

Other technology requirements / equipment / material

You will be **required** to bring a wireless laptop to all classes.

Course Requirements and Assignments

- Each student is expected to be present, punctual, and prepared at every scheduled class and lab session. It is assumed that the students already have basic knowledge of digital Boolean logic and fundamentals of assembly language machine programming.
- Attendance is **NOT** optional. Individual participation is also required. There will be no make-ups for missed midterm or assignments, unless any special arrangements is made with the instructor beforehand.
- All student **must complete** the ***Syllabus agreement*** through by ***Jan 31, 2017 11:59 pm***. Any one **failed** to do so will be **dropped** from the class. This agreement will be sent to individual email as '***CS147-SP17-PreReq-Survey***' in https://sjsu.qualtrics.com.
- There will be **3 home works, 3 individual project,** one **midterm** and **final exam**. All home works and projects should be submitted through Canvas. **No scanned copy** of handwritten solution is allowed. Allowed document type is **PDF** only.

Project report should contain the following.

- Introduction containing objective.
- Requirement.

- Design and Implementation.
- Testing
- Conclusion
- Make sure to
  1. Include clear diagrams for requirement and design.
  2. Include code snippet to explain implementation.
  3. Include screen shots of testing results.
  4. Upload source code and test program as zip archive.

Project reports are encouraged to be submitted in IEEE format.
[http://www.ieee.org/conferences_events/conferences/publishing/templates.html]

10% of the obtained marks in project will be awarded as extra points in project evaluation if report submitted in proper IEEE format.

Final Examination or Evaluation

There shall be an appropriate final examination and evaluation at the scheduled time as indicated in University calendar, unless specifically exempted by the college dean who has curricular responsibility of the course. The examination is expected to have descriptive, problem analysis and problem solving style questions to answer.

Grading Information

1. Homework carries **30%** towards final score. Average of 3 score from homework will be contributed.
2. Project carries **30%** towards final score. Average of 3 score from projects will be contributed.
3. Midterm carries **20%** towards final score.
4. Final carries **20%** towards final score.

Submission is allowed till **11:59 pm on due date**. Zero delay tolerance for the submission, i.e. NO late submission is permitted, unless you make special arrangements with your instructor beforehand.

You will receive a numeric score for the midterm, the final, each of the total homework, and each project submission. Letter grade, which is your class grade, will be obtained by adding the numeric scores and weighing with the percentages given below. Fraction in percentage will be converted into nearest integer value ('>= 0.5' will be moved to next integer number, '< 0.5' will be moved to previous integer number).

A+ = 100-97%	A = 96-93%	A- = 92-90%
B+ = 89-87%	B = 86-83%	B- = 82-80%
C+ = 79-77%	C = 76-73%	C- = 72-70%
D+ = 69-67%	D = 66-63%	D- = 62-60%
F = 59-0% Failure		

Classroom Protocol

1. **You must come to class on time!** Students entering the classroom late disrupt the lecture and / or the students already in class who may be engaged in lab or discussion. Late students will not be accepted in class.

2. If you miss a lecture you are still responsible for any material discussed or assignments given. A large portion of each class will be used for hands-on lab / discussion. All students are expected to participate in class activities. Students who are often absent will find themselves at a disadvantage during the tests.

3. No audio / video recording or photography in the classroom without prior permission of instructor.

4. It is individual **student responsibility** to **check validity** of their homework, assignment, project, submission (format error, blank files, corrupted files, and many more such) and re-submit within deadline if needed. Once the grading is started there will be no consideration for resubmit. ***If the submission found to have any logistics issue at grading time (format error, blank files, corrupted files, and many more such) it will be evaluated as 0***.

5. No personal discussion or cell phone activity during class time. Please set the cell phone on **silent/vibrate** mode.

6. All e-mail communication to the instructor must have the subject line start with **[CS147,01]**

7. Email to be sent to the instructor's SJSU email ID (kaushik.patra@sjsu.edu) only.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

Course Schedule – *subject to change by instructor with due notice.*

Date	Lecture	Lab	Notes
01/26/17	Intro CS147		
01/31/17	Introduction to Computer, Basic Instruction Set, ALU	Tool setup	HW01 / Project I Posted **Submit Prerequisite Survey & Syllabus Agreement**
02/02/17	Clock, Memory, Controller, Von-Neumann Architecture, System Software	Simulation Project	
02/07/17	Digital Synthesis, Number, Representation	Hierarchical Models	
02/09/17	Boolean Algebra I	Data Flow Modeling I	Add code will be supplied through e-mail
02/14/17	Boolean Algebra II	Data Flow Modeling II	Project II Posted
02/16/17	Comb / Seq Logic I	Memory Modeling	HW02 Posted
02/21/17	Comb / Seq Logic II	Project II Discussion	**Project I Submission**
02/23/17	Seq Logic Design, Common Digital Components I	Behavioral Modeling I	**HW01 Submission**
02/28/17	Common Digital Components II	Behavioral Modeling II	**Project II Milestone 1 Submission**
03/02/17	Addition / Subtraction Logic Circuit	Behavioral Modeling III	
03/07/17	Multiplication / Division Logic Circuit	Behavioral Modeling IV	**Project II Milestone 2 Submission**
03/09/17	Putting Together a Microprocessor – I	Project II	
03/14/17	Putting Together a Microprocessor – II	Project II	**Project II Milestone 3 Submission**
03/16/17	Midterm Review	Project II	
03/21/17	**Midterm Exam**		
03/23/17	Instruction Set Architecture, RISC/CISC	Project II	**Project 02 Milestone 4 Submission**
03/28/17	**Spring Recess**		
03/30/17			
04/04/17	Processor Performance Measurement	Project II	Project III Posted
04/06/17	Pipeline Architecture I	Gate Level Modeling I	**Project II Submission**
04/11/17	Pipeline Architecture II	Gate Level Modeling II	
04/13/17	ILP, Hardware Threading	Gate Level Modeling III	HW03 Posted
04/18/17	Parallel Processing I	Project 03 Part I	**HW02 Submission**
04/20/17	Parallel Processing II	Project 03 Part II	
04/25/17	Memory Hierarchy, Cache Memory I	Project 03 Part III	
04/27/17	Cache Memory II	Project 03 Part IV	
05/02/17	Cache Memory III	Project 03 Part V	
05/04/17	Cache Memory IV	Project 03 Part VI	
05/09/17	Virtual Memory		**HW03 Submission**
05/11/17	Review I		**Project III Submission**
05/16/17	Review II		
05/18/17	**Final Exam @ 5:15 PM – 7:30 PM (DH351)**		