San José State University
Computer Science
CS 147 *Computer Architecture 02*, Fall 2017

Course and Contact Information

Instructor: Dr. Juan Gomez

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Office Hours: Thursday 4:55-5:55pm *[See University Policy S12-1 at http://www.sjsu.edu/senate/docs/S12-1.pdf for faculty office hours guidelines]*

Class Days/Time: TTh 7:30-8:45am

Classroom: MH 225

Prerequisites: CS 47 Introduction to Computer Systems or CMPE 102 Assembly Language Programming with C- or better.

Course Format

Technology Intensive, Hybrid, and Online Courses

Students must access to the internet and Canvas for this class. Most material will be posted there and students will also be required to turn in programming projects online. See University Policy F13-2 at http://www.sjsu.edu/senate/docs/F13-2.pdf for more details.

Faculty Web Page and MYSJSU Messaging (Optional)

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on my class web page in Canvas (https://sjsu.instructure.com). You are responsible for regularly checking with the messaging system to learn any updates.

Course Description

"Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy."

GE Learning Outcomes (GELO)

Upon successful completion of this course, students should be able to:

• SLO 1 Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.

• SLO 2 Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.

• SLO 3 Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.

• SLO 4 Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.

• SLO 5 Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.

• SLO 6 Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.

• SLO 7 Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.

• SLO 8 Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.

• SLO 9 Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.

• SLO 10 Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.

• SLO 11Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware designs.

Course Learning Outcomes (CLO) (Required)

- CLO1 Review the basic Boolean number representation schemes, digital logic gates, and basic combinatorial and sequential circuit structures.
- CLO2 Introduction to the basic roles and responsibilities for each of the major hardware components of a computer.
- CLO3 Review the need to use a memory hierarchy, perform memory management, and to explain to them the various memory management techniques and their tradeoffs.
- CLO4 Review implementation of the fundamental mathematical operations such as addition, subtraction, multiplication, and division and optimization with Boolean operands.
- CLO5 Review tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).
- CLO6 Review non-classical architectures such as parallel processors and pipelined machines which are used to accelerate hardware performance without impacting legacy sequential software programming languages or techniques.
- CLO7 Introduction to computer-aided design tools and hardware description languages useful to computer architects in performing functional verification and performance measurements of digital systems.
- CLO8 Review operation of hardware and software working synergistically together.

Required Texts/Readings

Textbook

David A Patterson and John L. Hennessy
***ARM Edition**, Publisher: MK/Elsevier*

ISBN 978-0-12-801733-3

Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on.
More details can be found from University Syllabus Policy S16-9 at http://www.sjsu.edu/senate/docs/S16-9.pdf.

Final Examination or Evaluation

Final Exam (Thursday, December 14, 2017 @ 07:15-09:30am) 35%
(See Final Exam Schedule at http://info.sjsu.edu/static/catalog/final-exam-schedule-fall.html)

Grading Information (Required)

1.-Quizes / Homework (~ bi-Weekly) 30%
2.-Midterm-1 (Tuesday 10/03/2017, during class time) 15%
3.-Midterm-2 (Thursday 11/16/2017, during class time) 20%
4.-Final Exam (Thursday 12/14/2017 @ 07:15-09:30am) 35%

Determination of Grades

No make-ups exams except in case of verifiable emergency circumstances; once you are back in school, you need to take the exam within a week assuming that you provide documents to justify your absent and it is for a short time. No credit for any late turnings.

Grades will be assigned as described below in a system where the maximum grade is 100 points.

· A+: [97, 100]
· A: [93, 97)
· A-: [90, 93)
· B+: [82, 90)
· B: [75, 82)
· B-: [65, 75)
· C+: [60, 65)
· C: [55, 60)
· C-:[50,55)
· D+:[42, 50)
· D: [35, 42)
· D- :[25, 35)
· F: [0, 25)

Important: As an example, a student with a final grade of 96 / 100 will have a letter grade of A (not A+). I.e. no special handling of border situations will be performed and the grading scale above will be followed strictly.

Classroom Protocol

See class policies to be posted in the class website.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

CS 147 / *Computer Architecture* / Fall 2017, Course Schedule

(schedule is subject to change with fair notice via the class website).

Date	***Topic***	***Textbook Chapter***
08/24/2017	*Administrative*	
08/29/2017	*Computer Abstraction and Technology*	*Chapter 1*
09/12/2017	*Instructions: Language of the Computer*	*Chapter 2*
09/26/2017	*Arithmetic for Computers*	*Chapter 3*
10/03/2017	*Midterm 1*	
10/10/2017	*The Processor*	*Chapter 4*
10/31/2017	*Large and Fast: Exploiting Memory Hierarchy*	*Chapter 5*
11/16/2017	*Midterm 2*	
11/21/2017	*Parallel Processors from Client to Cloud*	*Chapter 6*
12/14/2017	***Final Exam***	07:15-09:30

Important NOTE:

In rare occasions, the instructor may decide to administer evaluations where students are allowed to use their "paper notes"-(NO BOOK OR ELECTRONIC COPIES), so it is in your best interest to attend to class and take good notes; they may be handy in such situations.