San José State University
Computer Science Department
CS 147, Computer Architecture, Section 3, Fall 2018

Course and Contact Information

Instructor:	Dr. Faramarz Mortezaie
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Office Hours:	T TH 7:30 AM - 8:00 AM room ENG-337
Class Days/Time:	MW 9:00 - 10:15 AM
Classroom:	MH-422
Prerequisite:	CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)

Course Format
Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas Leaning Management System course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through MySJSU at http://my.sjsu.edu (or other communication system as indicated by the instructor) to learn of any updates.

Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Learning Objectives (CLO)

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.
- Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware design

Required Texts/Readings Textbook

COMPUTER ORGANIZATION and DESIGN – The Hardware/Software Interface |

Edition: 5th *David A Patterson and John L. Hennessy* ***ARM Edition****, Publisher: MK/Elsevier*

ISBN 978-0-12-801733-3

Other Readings

COMPUTER ORGANIZATION and ARCHITECTURE | Edition: 10th Author: Stallings
ISBN: 9780134101613
Publication Date: 01/12/2015 Publisher: PEARSON

Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in University Policy S12-3 at http://www.sjsu.edu/senate/docs/S12-3.pdf.

Homework, Midterm and Final exam are expected for this class. Homework is due on Canvas by class starting time on the due date. Each assigned problem requires a solution and an explanation (or work) detailing how you arrived at your solution. Cite any outside sources used to solve a problem. When grading an assignment, I may ask for additional information.

NOTE that University policy F69-24 at http://www.sjsu.edu/senate/docs/F69-24.pdf states that "Students should attend all meetings of their classes, not only because they are responsible for material discussed therein, but because active participation is frequently essential to insure maximum benefit for all members of the class. Attendance per se shall not be used as a criterion for grading."

Grading

Homework and project	25%
Exam-1	25%
Exam-2	25%
Comprehensive Final Exam	25%

The final and exams have fixed dates and can only be taken in the classroom during class time. Makeup exams will only be given in cases of illness (with signed documentation from a medical facility – original copy). Exams are closed book, closed notes, closed neighbor and comprehensive. The final exam is cumulative.

Course Grading Standards

A+	98 – 100%
A	93 – 97%
A-	90 – 92%
B+	88 – 89%
B	83 – 87%
B-	80 – 82%

C+	78 – 79%
C	73 – 77%
C-	70 – 72%
D+	68 – 69%
D	63 – 67%
D-	60 – 62%
F	59% and less

Note that "All students have the right, within a reasonable time, to know their academic scores, to review their grade-dependent work, and to be provided with explanations for the determination of their course grades." See University Policy F13-1 at http://www.sjsu.edu/senate/docs/F13-1.pdf for more details.

Classroom Protocol

Students are expected to participate all the lectures. Please turn off your cell phones during the lecture time.

University Policies

University Policies Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

CS147 / Computer Architecture, Fall 2018, Course Schedule

This schedule is subject to change. Any change will be communicated via Canvas with fair notice.

Course Schedule

Week	Date	Topics	Reading Assignments and homework	Due Date
1	08/22/18	Introduction	Class Notes	
2 2	08/27/18 08/29/18	Computer Abstractions and Technology Instructions: Language of the Computer	Chapter-1 Homework-1	9/05
3 3	09/03/18 09/05/18	No class, Labor Day-Campus Closed Instructions: Language of the Computer	Chapter-2 Homework-2	9/12

4 4	09/10/18 09/12/18	Instructions: Language of the Computer Instructions: Language of the Computer	Chapter-2 Homework-3	 9/19
5 5	09/17/18 09/19/18	Instructions: Language of the Computer Instructions: Language of the Computer	Chapter-2 Homework-4	 9/26
6 6	09/24/18 09/26/18	Arithmetic for Computers Arithmetic for Computers	Chapter-3 Homework-5	 10/08
7 7	10/01/18 10/03/18	Review Exam-1	Chapters 1 to 3	
8 8	10/08/18 10/10/18	Arithmetic for Computers Arithmetic for Computers	Chapter-3 Homework-6	 10/17
9 9	10/15/18 10/17/18	Arithmetic for Computers The Processor	Chapter-3 Chapter-4	
10 10	10/22/18 10/24/18	The Processor The Processor	Chapter-4 Homework-7	 10/31
11 11	10/29/18 10/31/18	The Processor The Processor	Chapter-4 Chapter-4 Homework-8	 11/12
12 12	11/05/18 11/07/18	Review Exam-2	Chapters 3 and 4	
13 13	11/12/18 11/14/18	No Class, Veteran's Day-Campus closed, Large and Fast: Exploiting Memory Hierarchy	Chapter-5 Homework-9	 11/21
14 14	11/19/18 11/21/18	Large and Fast: Exploiting Memory Hierarchy No Class,	Chapters 5 Homework-10	 11/28
15 15	11/26/18 11/28/18	Large and Fast: Exploiting Memory Hierarchy Large and Fast: Exploiting Memory Hierarchy	Chapter-5 Homework-11	 12/05
16 16	12/03/18 12/05/18	Parallel Processors from Client to Cloud Parallel Processors from Client to Cloud	Chapter-6	
17 **Final Exam**	12/10/18 12/12/18	Review (Wednesday) Final Exam	Chapters 1 to 6 7:15 – 9:30 AM (Friday)	