San José State University
Computer Science Department
CS247, Advanced Computer Architecture, Section 1, Fall 2016

Course and Contact Information

Instructor:	Robert Chun
Office Location:	MH 413
Telephone:	(408) 924-5137
Email:	Robert.Chun@sjsu.edu
Office Hours:	MW 4:30pm-5:30pm
Class Days/Time:	MW 1500-1614
Classroom:	MH422
Prerequisites:	CS147

Faculty Web Page

The term paper formatting template can be found on my faculty web page at
http://www.sjsu.edu/people/Robert.Chun/courses

Course Description

Detailed analysis of high-performance, fault-tolerant computer systems. Survey various machine architectures including implementation alternatives for major processor sub-systems. Pipelined, vector, VLSI, multi-core and dataflow architectures are examined. Discussion includes data representation, arithmetic logic unit operations and algorithms, rounding algorithms, control unit operation and instruction formats. Performance measurement and speedup techniques are studied to perform tradeoff analysis and design optimization. Digital breadboard labs and programming projects with the VHDL language and simulation environment will be used to demonstrate computer-aided design and functional verification techniques for digital systems. A written report and oral presentation on a relevant and approved topic of interest to the student will be required.
Insert course description from the University catalog augmented by section-specific description.

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

- Understand combinatorial and sequential circuit structures and Boolean number representation schemes
- Appreciate how the fundamental core mathematical operations such as addition, subtraction, multiplication, and division can be optimized with appropriate number representation, rounding, and digital circuit implementation schemes.
- Explain the tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).
- Discuss non-classical architectures such as parallel processors, multi-core chips, pipelined and VLIW machines which are used to accelerate hardware performance without impacting legacy sequential software programming languages or techniques.
- Emphasize the importance of fault-tolerant design techniques and examine various methods of error detection and correction such as TMR and Hamming Codes.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Utilize computer-aided design tools and hardware description languages useful to computer architects in performing functional verification and performance measurements of digital systems.
- Use industrial-grade field programmable gate array chips and their associated CAD toolsets.
- Appreciate how hardware and software (especially the operating system and compilers) must work synergistically together to provide optimum throughput.
- Perform an in-depth investigation of an architecture related topic of interest to them and present their findings to their classmates in an oral and written report using a venue similar to that used in formal professional technical conferences.

Required Texts/Readings

Textbooks

Computer Organization and Design: The Hardware/Software Interface, 4th Ed., Revised Printing, D. Patterson, 2009, Morgan Kaufmann, ISBN 9780123744937

A VHDL Primer, J. Bhasker, 3rd Ed., 1999, Prentice Hall, ISBN 9780130965752

CS 247 Course Reader, Chun. Purchase at SJSU AS Print Shop.

Course Requirements and Assignments

Assignments include two midterms, one final, a written and oral report, and a set of projects (consisting of a combination of written problems and VHDL programming assignments) weighted as shown below. Grading is based on a class curve. All assignments (especially the oral presentation) must be completed by the student on the due date specified to receive credit for the class. Late assignments or exams are not accepted. All students must uphold academic honesty, especially for the required term paper, per university policy detailed at http://www2.sjsu.edu/senate/f88-10.htm

Final Examination

The final exam for the class will be held on Monday, December 19, 2016 at 1215-1430.

Grading Information

Grading consists of two midterms, one final, a written and oral report, and a set of projects (consisting of a combination of written problems and programming assignments) weighted as follows. Grading is based on a class curve. All assignments (especially the oral presentation) must be completed by the student on the due date specified to receive credit for the class. Late assignments or exams are not accepted. All students must uphold academic honesty, especially for the required term paper, per university policy detailed at http://www2.sjsu.edu/senate/f88-10.htm

15% Midterm Exam 1
Week 6 (Approximate)

15% Midterm Exam 2
Week 12 (Approximate)

30% Term Paper/Project & Presentations
Weeks 13-15

30% Final Exam
December 19, 2016 at 1215-1430.

10% Combined total of Three HW/and VHDL Projects
Due as announced in class

Classroom Protocol

Students are expected to attend all classes.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

CS247 Fall 2016 Tentative Course Schedule

Lecture	Chapter	Topic
1-4	1, 2	Introduction, VHDL
5-6	3	Data Representation
7-10	3	High Speed Computer Arithmetic

11	Notes	Rounding
		Midterm Exam
12-16	6	Pipeline and Parallel Processing
17-21	Notes, Readings	Fault-Tolerance
		Midterm Exam
22-27		Term Papers & Oral Presentations

Final Exam Monday, December 19, 2016 at 1215-1430.