COMPREHENSIVE EXAM STUDY GUIDE

ELECTRICAL ENGINEERING
SAN JOSE STATE UNIVERSITY

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EE 223 - Analog Integrated Circuits

Students will be tested on topics such as nanoscale metal-oxide semiconductor field effect transistor (MOSFET) modeling and circuit design techniques for analog integrated circuit applications. Exam topics might include short channel design issues, device mismatch and layout techniques to improve design performance, noise modeling and transformation, high-swing current mirrors, bandgap, gain, bandwidth and voltage swing characteristics of single-stage and two-stage amplifiers. Good knowledge of opamp architectures with their slew rate, settling time, phase margin, stability, gain and bandwidth are required.

Reference Textbook: Exam will cover Chapter 2-6 and Chapter 9-11 of the following textbook.

Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw Hill, 2001.

Topics that will be tested include:
- Biasing Short-Channel MOSFETs
- Small-Signal Modeling of MOSFETs
- DC Error and High Frequency Modeling of Current Mirrors
- MOSFET mismatch and Current Mirror mismatch
- Common Gate Av0, ωp1, ωp2, ωz , Rin, Rout Calculations
- Common Source Av0, ωp1, ωp2, ωz , Rin, Rout Calculations
- Common Drain Av0, ωp1, ωp2, ωz , Rin, Rout Calculations
- Source Degeneration Av0, ωp1, ωp2, ωz , Rin, Rout Calculations
- Cascode Av0, ωp1, ωp2, ωz , Rin, Rout Calculations
- Differential-Pair Av0, ωp1, ωp2, ωz , Rin, Rout Calculations
- Bandgap circuit operation
- Opamp Frequency Compensation and Pole Splitting
- Opamp Voltage Swing and Slew Rate
- Estimating Resistance and Capacitance at any Node of any Circuit

EE 224 - High Speed CMOS Circuits

Main reference "Digital Integrated Circuit, Jan Rabaey, Prentice Hall, 2nd Edition." Chapter 2, 3, 5, 6, 7

1. Diode
    a. Model
    b. Operation
    c. Circuit based on Diode

2. MOSFET
    a. Model and Structure
    b. Operation Modes
    c. Circuit based on MOSFET

3. Combinational Circuits
    a. Inverter
        i. Active load
        ii. CMOS
    b. Buffer Chain Design

4. Sequential Circuits
    a. Sequential CMOS Circuit
    b. Latch Design
    c. Flip-Flop Design

5. Logical Effort, Electrical Effort
6. SRAM Design
7. Timing

EE 287 - ASIC CMOS Design

1. CMOS Gate Review

1.1 What is VOH, VOL, and VM?
1.2 What is symmetrical CMOS?
1.3 How are switches arranged to form the AND function?
1.4 How are switches arranged to form the OR function?
1.5 What is a CMOS pass switch?
1.6 What is a Tri-State gate?

2. Latches

2.1 Draw schematics for a CMOS NAND based latch
2.2 Draw schematics for a CMOS mux based latch
2.3 Draw schematics for a CMOS pass gate based latch
2.4 Make a rising edge triggered D flip-flop
2.5 Make a falling edge triggered JK flip-flop with reset and clear
2.6 Explain Master/Slave flip-flop operation.
2.7 Add reset and clear to any of the above flip-flops
2.8 Add synchronous reset to any of the above flip-flops
2.9 What is a meta-stable state? What can be done to design around it?
2.10 What precautions should be taken when sending signals between flip-flops on different clocks?
2.11 What are the differences between gated and re-circulating flip-flops? What are the impacts on clock and long path timing?

3. ASIC Concepts

3.1 Why is it important to have products to market early?
3.2 Calculate if a product should use an ASIC, FPGA, or custom chip. (Like homework assignment)
3.3 What type of product is best for stable markets with huge volumes.
3.4 What type of product is best for quick time to market and very small volumes.
3.5 What type of product is best for medium volumes, and good time to market.
3.6 What parts of the silicon design does the ASIC vendor normally perform? Which parts do we perform as ASIC engineers?
3.7 What factors need to be satisfied to have a successful product? How can you ensure they are met?
3.8 Why are there design rules for ASIC engineers? What do they help in the ASIC process? List 3 such rules.

4. ASIC Delay

4.1 What are the two major contributors to loads in ASICs?
4.2 What is the simple ASIC delay model? Extract numbers from a data sheet, and use to solve problems.
4.3 Calculate the delay for an ASIC gate.
4.4 Calculate the short and long path for a small ASIC network of gates. (Like homework assignment)
4.5 Improve the delay in an ASIC network by rearranging inputs on gates.
4.6 Why do the libraries have different types of cells with the same function? Use different cells to change network timing.

EE 287 - ASIC CMOS Design (cont'd)

4.7 Why doesn't CMOS make single level 8 input NAND gates? How does the area required grow as the height of the transistors increases?
4.8 Why are NAND gates preferred to NOR gates in most CMOS ASIC design?
4.9 Why will timing only be "estimated" until physical design is complete?

5.synthesis

5.1 Why does the library have so many and- or/invert cells?
5.2 What steps does the synthesis software use in arriving at the final gates in the ASIC?
5.3 What does the synthesis routines do to attempt to achieve timing?
5.4 What constraints need to be provided to the synthesis software for effective timing synthesis?

6. Cycle Time

6.1 What is input setup time?
6.2 What is input hold time?
6.3 What is clk->Q time (Sometimes called output hold time)
6.4 What is the relationship between data, clk setup/hold, and clk->Q time that must be met if there is to be no long path in the design?
6.5 What is the relationship between data, clk setup/hold and clk->Q time that must be met if there is to be no short (race) path in the design?
6.6 Analyze a circuit to determine if there is a race or long path.
6.7 What is the impact of clock skew on short and long paths?
6.8 Draw a timing picture with clock skew, setup, hold, and clk->Q times for a cycle time indicating the amount of time for logic in a long path, and the amount of pad (if any) in a short path.
6.9 Trace the time through a network starting with clock skew.
6.10 What is the duty cycle of a clock. Does it matter if the clock is edge triggered?
6.11 Which clock edge is better? Which is most commonly used in industry? Should all flip-flops use the same edge unless function required otherwise? Why or Why not?

7. Quick timing fixes

7.1 List 4 quick timing fixes. Explain how each can improve timing.
7.2 Re-order a logic expression to synthesize faster.
7.3 What cell substitutions can result in less delay?
7.4 Why should hierarchy blocks not bee too small?
7.5 What happens if all the cells in a design become larger?
7.6 How can select faster cells improve a long path?
7.7 Why is the cycle time often set shorter than desired? How does this help the long path problems? What are the negatives?
7.8 When in the design cycle should long path problems be discovered? Why?

8. Block communications

8.1 What is pipelining? How does it result in a higher clock frequency?
8.2 What is the 1 flag push model for block communications?
8.3 What is the 1 flag pull model for block communications?
8.4 Why are flag based block communications models used? What benefit do they provide?

EE 231 - Automatic Control Theory

The exam covers the following topics.

- Analysis of systems described by block diagrams (block diagram simplification, overall transfer function, DC gain, frequency response etc.)
- PID controller
- Nyquist criteria and compensation (Bode plot, lead-lag compensator, phase and gain margin etc.)
- State space representation (transition matrix, etc.)
- Realization and canonical forms
- Controllability and observability
- Full-state feedback controller
- Observer-based state feedback controller
- Reduced-order estimator

The exam problems can be of the type of question-and-answer and/or analysis. You will need a scientific calculator for the analysis problems. The analysis problems will be numerically simple. For example, you will not be expected to invert a 3x3 matrix or to find the roots of a polynomial of 3rd or higher order.

Reference book: Feedback Control of Dynamic Systems. Franklin, Powell, and Emami-Naeini. Addison Wesley. 6th or 7th Edition. (For this exam, you can use any edition of this book as a study guide.)

EE 238 - Advanced Power Electronics

The exam covers the following topics.

- Analysis of switch mode converter topologies.
- Analysis of PWM rectifiers/inverters.
- Principles of steady state converter analysis
- Steady state equivalent circuit modeling, losses, and efficiency.
- Converter transfer function, state space averaging
- Continuous/discontinuous conduction modes of operation.
- Voltage mode/current mode control.
- Modulation strategies.
- Applications to grid tied/grid interactive photovoltaic inverters.

- The exam problems can be of the type of question-and-answer and/or analysis. You will need a scientific calculator for the analysis problems.
- Reference book Power Electronics: Converters, Applications, and Design. Ned Mohan, Tore M. Undeland, William P. Robbins.

EE 251 - Digital Communication Systems

Introduction
The course EE251 covers the fundamentals of digital communication systems. It is expected that the student will understand the process of mapping bits to signal waveforms, evaluate the effects of Gaussian noise on system performance and of bandlimited channels on the received waveforms, and the processes of matched filtering and statistical decision that are required in order to remove interference and minimize the probability of a bit error given a signal-to-noise ratio.

Study material
The student shall be able to understand, derive and manipulate the mathematical principles and the applications of each of the following topics.

1. Mapping via a signal constellation
    a. Signal space and signal points
    b. Bits-to-signals mapping
    c. Relation between signal points and waveforms
    d. Average signal energy and its relation to average bit energy
2. Matched filter (MF)
    a. Intersymbol interference (ISI)
    b. Filter design for removal of ISI
    c. Raised-cosine spectrum
3. Maximum-likelihood decision rule
    a. Sampled MF outputs of waveforms with AWGN: Decision variables
    b. Decision boundaries in the signal space
    c. Decision rule based on maximum likelihood
4. Average probability of error
    a. Average probability of a symbol error
    b. Approximated probability of a bit error from the bits-to-signal mapping
    c. Derivation and computation of these probabilities using the Gaussian Q-function

All this topics are covered in the textbook below. However, other textbooks may be used to study. Each of the topics above shall be applied to any of the following (linear) constellations:

- Binary phase-shift keying – BPSK
- Quaternary phase-shift keying – QPSK
- M-ary phase-shift keying – M-PSK
- M-ary quadrature amplitude modulation – M-QAM

Modulations such as M-FSK, MSK or OFDM are covered in the EE252 course. In the exam, typically a small constellation selected from the set above will be given in a problem. Any formula needed will be provided in the exam. If no formula is given then it is expected that the student will derive it during the exam.

Textbook S. Haykin, *Communication Systems,* 4th Ed., Wiley, 2001.

EE 253 - Digital Signal Processing I

1. Time and frequency analysis of discrete-time signals and systems

2. Various Transforms
   a) Fourier Transform (FT)
   b) Fourier series (FS)
   c) Discrete Time Fourier Transform (DTFT)
   d) Z transform
   e) Discrete Fourier series (DFS)
   f) Discrete Fourier Transform
   g) Fast Fourier Transform
   h) Convolution
   i) Sampling process

3. Design and implementation of FIR filters (LP, HP, BP, BS, Hilbert-transformers, differentiators) using the window and optimal algorithms.

4. Design and implementation of IIR filters based on analog filter prototypes and the bilinear transformation.

5. Spectral analysis of deterministic signals. Spectral resolution and leakage

6. Analysis of various classical discrete-times filters (LP, HP, BP, BS, comb, notch, multi- notch, allpass filters).

7. Multi multirate signal processing: decimation, interpolation, and sample rate conversion.

8. Implications of quantization effects on digital filter design rate signal processing: decimation, interpolation, and sample rate conversion. Efficient implementations.

EE 257 - Machine Learning for EE
(or EE 258 - Neural Networks)

Note: *If you have taken either EE257* ***or*** *EE258, you should be able to answer the comprehensive exam question.*

- Textbook A: *An Introduction to Statistical Learning with Applications in R , Springer 2013, By: G. James, D. Witten, T. Hastie, and R. Tibshirani. ISBN-10: 1461471370.*
- Textbook B: *Hands-On Machine Learning with Scikit-Learn &TensorFlow by Aurelien Geron, O'Reilly Media, April 2017.* ISBN-10: 1491962291 ISBN-13: 978-1491962299 *(available in library in digital format)*

Topics: machine/statistical learning basics, underfitting, overfitting, linear regression, classification , performance metrics (MSE, R^2, Accuracy, Precision, Recall, Confusion Matrix, ROC, etc), Regularization (Ridge (L^2-norm), Lasso (L^1-norms)), Unsupervised Learning (K-means)

Sections from the textbook A:
Chapter 2 (2.1, 2.2)
Chapter 3 (3.1,3.2, 3.3)
Chapter 4 (4.1, 4.2, 4.3)
Chapter 6 (6.2)
Chapter 10 (10.3.1)

Sections from the textbook B:
Chapter 1 (Pages 3-13, 23-30)
Chapter 3 (Pages 81-102)
Chapter 4 (Pages 107-113, 124, 130-133, 137-142)

EE 270 - Advanced Logic Design

I. Review of switching algebra
- Boolean arithmetic and switching function fundamentals
- Axioms and theorems, maxterm and minterm theorems

II. Automation of switching function simplifications
- Quine-McCluskey method (base-line, incompletely specified, multiple-output)
- Espresso Algorithm (reduction, expansion, irredundant operation in PCN)

III. Synchronous circuit design
- Sequential devices (latches and flips/flops)
- Analysis and synthesis of synchronous sequential circuits
- State reduction of completely and incompletely specified circuits
- Optimal state assignment methods

IV. Asynchronous sequential circuits
- Analysis and synthesis of Huffman Circuit (fundamental mode)
- Race and cycles
- Critical race avoidance methods

Note: Due to the fact that the exam usually takes place a few weeks before the end of the semester. Additional topics such as Muller Circuit and Design for Testability will NOT be covered by the exam question.

EE 271 - Digital System Design and Synthesis

Students will be tested on topics related to combinational and sequential digital circuit design and optimization, Verilog HDL, static timing analysis and dynamic timing analysis

Reference Materials: EE271 lecture notes #2, #3, #4, #5, #6 and #7

Topics that will be tested include:

- Boolean algebra, Demorgan's laws, Shannon's expansion
- Two-level and multi-level combinational circuits
- Optimizing combinational circuits - Boolean cubes, K-maps (up to 4 variables)
- Hazards and glitches
- Finite state machine implementations and optimizations (D-flipflops only)
- Implementing and verifying digital circuits with Verilog HDL
- Static timing analysis - timing paths, timing constraints, clock skews, clock jitters, false paths
- Dynamic timing analysis – gate-level timing simulation

EE 275 - Advanced Computer Architectures

- MIPS instruction set architecture, addressing, and control sequencing; performance measure
- MIPS pipeline hazards and techniques to enhance ILP; Superscalar pipeline and scheduling techniques including scoreboarding and Tomasulo's algorithm
- Basic concept of DLP, vector processor, array processor
- Cache memory system and design; cache coherence in multiprocessor
- Virtual memory and TLB
- Basic concept of Thread-Level Parallelism and multiprocessor; Basic concept of Request- Level Parallelism and Warehouse-scale computer for data center

EE 281 - Internetworking

The Comprehensive Exam for EE 281 will cover the following:

- Protocol Layering Concepts, TCP/IP Protocol Suit, OSI Model

- Data Link Layer:
  - Ethernet and IEEE 802 project
  - Framing, Access Control, Error Detection (CRC)
  - Switching Hardware and Switch Fabrics, Crossbar, Banyan Switches

- Network Layer
  - Subnetting and routing, steps in sending IP packets (unicast, multicast)
  - Routing layer protocols (ARP, ICMP, RIP, OSPF)
  - IPv4, IPv6, packet formats* and addressing
  - Basic functionalities and structure of routers

- Transport Layer
  - Socket Addressing
  - Congestion and flow controls (Go-Back-N, Selective-Repeat Protocols)
  - UDP packet formats* and services
  - TCP packet formats* and services, Nagle's Algorithm and Silly Window Syndrome
  - TCP FSM (Slow Start, Fast Recovery, Congestion Avoidance, cwnd, ssthesh. MSS)
  - TCP Implementations: Taho, Reno

- Application Layer:
  - Layer service, client-server and peer-to-peer paradigms
  - HTTP: Message Format* (GET,HEAD, PUT, POST…), Request/Response messages, Cookies
  - FTP: Request/Response messages

(*) The protocol format will be provided in the exam, however students need to be able to determine the functionalities and purposes of each of its fields and segments.

EE 283 - Broadband Communication Networking

1. **Tunnels, VPNs, & MPLS Networks (Ch. 14)**
    - Tunneling
    - IPv6 Tunneling and Dual-Stack Lite
    - Virtual Private Networks (VPNs)
    - Multiprotocol Label Switching (MPLS)
    - Labels and Label Switch Routers (LSRs)
    - Label Binding and Switching
    - Routing in MPLS Domains
    - MPLS Packet Format
    - Multi-Tunnel Routing

2. **Optical Networks, GMPLS**
    - Generalized MPLS (GMPLS) Protocol
    - Passive Optical Networks (PONs)
    - Basic Optical Networking Devices
    - Optical Switches
    - Large-Scale Optical Switches
    - Structure of Optical Cross Connects (OXCs)
    - Blocking Estimation over Lightpaths

3. **Cloud Computing & Virtualizations (Ch. 16)**
    - Cloud Computing and Data Centers
    - Data Centers
    - Virtualization in Data Centers
    - Data Center Networks (DCNs)
    - Load Balancer
    - Traffic Engineering
    - DCN Architectures
    - Multicast Methods
    - Network Virtualization
    - Network Virtualization Components
    - Overlay Networks

4. **Architecture of Advanced Routers (Ch. 12)**
    - Control Plane
    - Router CPU
    - Routing Protocol Processor
    - Routing Tables
    - Congestion Control Processor
    - Data Plane
    - Input Port Processor (IPP)
    - Packet Parser

EE 283 - Broadband Communication Networking (cont'd)

- Packet Partitioner
- Input Buffer
- Routing Table (IPv4 and IPv6)
- Multicast Scheduler
- Forwarding Table and Packet Encapsulator
- Output Port Processor (OPP)
- Output Buffer
- Reassembler and Resequencer
- Error Control
- Switch Fabric
- Contention Resolution Unit
- Complexity of Switch Fabrics
- Crossbar Switch Fabrics
- Clos Switch Fabrics
- Concentration and Expansion Switch Fabrics
- Shared-Memory Switch Fabrics
- Performance Improvement in Switch Fabrics
- Multicasting Packets in Routers
- Tree-Based Multicast Algorithm
- Packet Recirculation Multicast Algorithm

5. Software Defined Networking (Ch. 17)

- Separation of Control and Data Planes
- Programmability of the Control Plane
- Application Programming Interfaces (APIs) SDN-Based Network Model
- Control Plane
- Data Plane Interface (OpenFlow Protocol)
- Small-Size SDN Architectures
- Scalability of SDN
- Multicasting in SDN-Based Networks
- SDN Architectures for Clouds
- Software-Defined Compute and Storage
- Application Delivery in Data Centers by SDN
- Network Functions Virtualization (NFV)
- Abstract Model of NFV
- Distributed NFV-Based Networks
- Virtualized Services
- Information-Centric Networking (ICN)
- Named Objects
- ICN Routing and Network Management
- Network Emulators for Advanced Networks
- Mininet

EE 286 - Wireless and Mobile Networking

1. Cellular Networks

- Calculate the distance between two cells, d, as a function of the range of each cell, r, based on the hexagonal pattern
- Calculate the distance between two co-channel cells, D as a function of r and the cluster size
- Learn the main components of a cellular network and their roles, including BSC, MSC, SGSN, Location Register, EnodeB, PGW, SGW, HSS, MME
- Describe how a call get established in 3G and LTE cellular networks
- Calculate the throughput of a network with a given carrier bandwidth, number of carriers, frequency reuse, and modulation scheme
- Understand the Mobile IP protocol

2. 802.11 WiFi

- Learn the steps in establishing communication using CSMA/CA, including SIFS, DIFS, RTS, CTS, and backo_ counters
- Calculate the throughput of 802.11 and learn what are the required parameters needed to make the calculation, including probability of collision and number of users
- Understand the concept of a Renewal-Reward process

3. Bluetooth and ZigBee

- Learn the 4 type of states of members in Bluetooth networks and their roles: Master, Slave, Stand-by, Park
- Know the medium access protocol used by Bluetooth: FH/TDMA/TDD
- Learn the types of members of ZigBee networks and their roles: FFD, RFD
- Know the medium access protocol used by ZigBee: CSMA/CA with beacons

4. Ad hoc Networks

- Be able to _nd the probability of a network being connected as a function of range and number of users in the network
- Answer the following question for each of the four Ad hoc routing protocol (DSDV, DSR, TORA, AODV):
    - What information does each node have?
    - What are they sharing?
    - When do they share it?
    - How are routes established?,
    - How many routes?,
    - How are routes maintained after a link failure?