

San José State University
Department of Electrical Engineering
EE-224, High Speed CMOS Circuits, Section 01, Spring, 2021

Course and Contact Information

Instructor:	Dr. Hiu Yung Wong
Office Location:	Online (Zoom)
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Email:	hiuyung.wong@sjsu.edu
Office Hours:	Mon: 9:00am-10:30am, Wed: 1:30pm-3:00pm, or by appointment
Class Days/Time:	Monday and Wednesday 3:00pm-4:15pm
Classroom:	Online (Zoom)
Prerequisites:	Graduate standing or instructor consent

Course Description

This course teaches the principles of high speed CMOS circuit design. Students will learn the metrics and their trade-off in high speed CMOS circuits, namely power, area, performance and cost. They will learn how to do first order analysis of basic components (diode, transistor, interconnect) by hand. Then circuit analysis techniques (such as logic effort) will be introduced which allow the students to select the best circuit topology to meet design criteria. CMOS inverter and other combinatorial logics will be emphasized. After that, arithmetic logic unit, which is the fundamental and building block of many high-speed CMOS circuits will be discussed. Students will also learn the design principles of advanced topics such as sequential logic, interconnect issue, timing issue, and memory. In this process students should gain intuition on various high-speed CMOS circuit designs through hand calculation. They will have opportunity to verify their intuition by implementing a high-speed circuit in the design project using commercial EDA tool.

Course Format

Technology Intensive and Hybrid Class

This class has 2 lectures per week. The students are expected to have stable internet access to attend the online lectures through Zoom. The students need to have Webcam installed on their computer and be able to use LockDown Browser by Respondus to take quizzes and exam. Their computers should be compatible to remote desktop to access the servers in the campus. **Please see the following for more details.**

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on [Canvas Learning Management System course login website](http://sjsu.instructure.com) at <http://sjsu.instructure.com>. You are responsible for regularly checking with your official email (the email address stored on your MySJSU account) and the messaging

system through [MySJSU](http://my.sjsu.edu) at <http://my.sjsu.edu> (or other communication system as indicated by the instructor) to learn of any updates.

Course Learning Outcomes:

CLO1: Understanding MOSFET and Diode circuit in large signal domain.

CLO2: Understanding transistor sizing for high speed logic gates.

CLO3: The ability to size transistors for high speed low power combinational logic.

CLO4: The ability to size transistors for high speed low power sequential circuits.

CLO5: Understanding the concept of buffer design.

CLO6: Understanding the concept of logical effort.

CLO7: The ability to run transistor level circuit simulation and layout circuits.

CLO8: Understand the trade-off between area, power, performance and cost.

CLO9: Understand how process variation and interconnect delay are playing more critical roles in high-speed CMOS design.

CLO10: Understand memory design.

Upon successful completion of this course, students will be able to:

1. *Demonstrate an understanding of the fundamentals of Electrical Engineering, including its mathematical and scientific principles, analysis and design.*
2. *Demonstrate the ability to apply the practice of Engineering in real-world problems.*

Required Texts/Readings

Textbook

Digital Integrated Circuit, Jan Rabaey, Prentice Hall, 2nd edition

<https://www.pearson.com/us/higher-education/program/Rabaey-Digital-Integrated-Circuits-2nd-Edition/PGM263532.html>

Other Readings

Low Power Design Essentials, Jan Rabaey, Springer; 2009 edition (April 13, 2009).

We have ordered e-copies and you can check out/download from our library through this link:

https://sjsu-primo.hosted.exlibrisgroup.com/primo-explore/fulldisplay?docid=01CAL5_ALMA71408235220002901&context=L&vid=01CAL5_SJO&search_scope=EVERYTHING&tab=everything&lang=en_US

Software

Cadence

Course Requirements and Assignments

Students are expected to attend all classes and participate actively in the seminar, submit the assignments and project reports on time and attend the mid-term and final exams. Assignments and Project Reports must be submitted on time to receive full credit. Late submission of Assignments and Project Reports within 3 days after the due date will only receive half of the credits. No credits will be given after the late submission due date.

Review the following policy about your responsibility:

- *Office of Graduate and Undergraduate Programs' [Syllabus Information web page](http://www.sjsu.edu/gup/syllabusinfo/) at <http://www.sjsu.edu/gup/syllabusinfo/>*

“Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus.”

Final Examination or Evaluation

Exams will be closed book. However, students are allowed to bring a calculator and a page of aid sheet. There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams. The course is based on letter grading and grading percentage breakdown is as follow:

Grading Information

Please also see Spring 2021 Special University Grading Policy (<https://www.sjsu.edu/registrar/academic-records/grade-changes.php>)

Assignment	15%
Midterm Exam-1	15%
Midterm Exam-2	15%
Final Exam	30%
Design Project	25%

Determination of Grades

- Every assignment has equal weight (totally 15% of the final score)
- Assignment and Project reports must be submitted on time to receive full credit. Late submission: Half of the credit will be given if submitted within 3 days after the due date. No credit will be given if submitted after late submission due date.

Grading Breakdown:

A = 100 to 93 points

A minus = 92 to 88 points

B plus = 87 to 84 points

B = 83 to 79 points

B minus = 78 to 75 points

C plus = 74 to 72 points

C = 71 to 69 points

C minus = 68 to 65 points

D plus = 64 to 62 points
D = 61 to 59 points
D minus = 58 to 55 points
F = 55 points or lower

Classroom Protocol

Students are required to be in class on time and no use of cell phone during the class.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' [Syllabus Information web page](http://www.sjsu.edu/gup/syllabusinfo/) at <http://www.sjsu.edu/gup/syllabusinfo/>"

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student's second offense in any course will result in a Department recommendation of suspension from the University.

Proctoring Software and Exams

Exams will be proctored in this course through Respondus Monitor and LockDown Browser. Please note it is the instructor's discretion to determine the method of proctoring. If cheating is suspected the proctored videos may be used for further inspection and may become part of the student's disciplinary record. Note that the proctoring software does not determine whether academic misconduct occurred, but does determine whether something irregular occurred that may require further investigation. Students are encouraged to contact the instructor if unexpected interruptions (from a parent or roommate, for example) occur during an exam.

Recording Zoom Classes

This course or portions of this course (i.e., lectures, discussions, student presentations) will be recorded for instructional or educational purposes. The recordings will only be shared with students enrolled in the class through Canvas. If, however, you would prefer to remain anonymous during these recordings, then please speak with the instructor about possible accommodations (e.g., temporarily turning off identifying information from the Zoom session, including student name and picture, prior to recording).

Students are not allowed to record without instructor permission

Students are prohibited from recording class activities (including class lectures, office hours, advising sessions, etc.), distributing class recordings, or posting class recordings. Materials created by the instructor for the course (syllabi, lectures and lecture notes, presentations, etc.) are copyrighted by the instructor. This university policy (S12-7) is in place to protect the privacy of students in the course, as well as to maintain academic integrity through reducing the instances of cheating. Students who record, distribute, or post these materials will be referred to the Student Conduct and Ethical Development office. Unauthorized recording may violate university and state law. It is the responsibility of students that require special accommodations or assistive technology due to a disability to notify the instructor.

Technology Requirements

Students are required to have an electronic device (laptop, desktop or tablet) with a camera and built-in microphone and speaker/headphone. SJSU has a free equipment loan program available for students.

Students are responsible for ensuring that they have access to reliable Wi-Fi during tests. If students are unable to have reliable Wi-Fi, they must inform the instructor, as soon as possible

or at the latest one week before the test date to determine an alternative. See Learn Anywhere website for current Wi-Fi options on campus.

Zoom Classroom Etiquette

1. Mute Your Microphone: To help keep background noise to a minimum, make sure you mute your microphone when you are not speaking.
2. Be Mindful of Background Noise and Distractions: Find a quiet place to “attend” class, to the greatest extent possible.
3. Avoid video setups where people may be walking behind you, people talking/making noise, etc.
4. Avoid activities that could create additional noise, such as shuffling papers, listening to music in the background, etc.
5. Limit Your Distractions/Avoid Multitasking: You can make it easier to focus on the meeting by turning off notifications, closing or minimizing running apps, and putting your smartphone away (unless you are using it to access Zoom).
6. Use Appropriate Virtual Backgrounds: If using a virtual background, it should be appropriate and professional and should NOT suggest or include content that is objectively offensive or demeaning.

Online Exams

Testing Environment: Setup

1. No earbuds, headphones, or headsets visible.
2. The environment is free of other people besides the student taking the test.
3. If students need scratch paper for the test, they should present the front and back of a blank scratch paper to the camera before the test.
4. No other browser or windows besides Canvas opened.
5. A workplace that is clear of clutter (i.e., reference materials, notes, textbooks, cellphone, tablets, smart watches, monitors, keyboards, gaming consoles, etc.)
6. Well-lit environment. Can see the students’ eyes and their whole face. Avoid having backlight from a window or other light source opposite the camera.
7. Personal calculator is allowed.

Testing Environment: Scan

Before students can access the test questions, they are expected to conduct a scan around their testing environment to verify that there are no materials that would give the student an unfair advantage during the test. The scan will include:

1. the desk/work-space

2. a complete view of the computer including USB ports and power cord connections
3. a 360-degree view of the complete room

Students must:

1. Remain in the testing environment throughout the duration of the test.
2. Keep full face, hands, workspace including desk, keyboard, monitor, and scratch paper, in full view of the webcam

Technical difficulties

Internet connection issues:

Canvas autosaves responses a few times per minute as long as there is an internet connection. If your internet connection is lost, Canvas will warn you but allow you to continue working on your exam. A brief loss of internet connection is unlikely to cause you to lose your work.

However, a longer loss of connectivity or weak/unstable connection may jeopardize your exam.

Other technical difficulties:

Immediately email the instructor a current copy of the state of your exam and explain the problem you are facing. Your instructor may not be able to respond immediately or provide technical support. However, the copy of your exam and email will provide a record of the situation.

Contact the SJSU technical support for Canvas:

Technical Support for Canvas Email: ecampus@sjsu.edu Phone: (408) 9242337
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If possible, complete your exam in the remaining allotted time, offline if necessary. Email your exam to your instructor within the allotted time or soon after.

EE-224 / High Speed CMOS Circuits, Spring 2021, Course Schedule***

***The schedule is subject to change with advanced notice on Canvas.

Week		Seminar	Reading	Assignment	Project
1	25-Jan	No Class			
	27-Jan	Quality Metrics of Digital Design	Ch. 1		
2	1-Feb	Fabrication Process	Ch. 2		
	3-Feb	Diode Models	Ch. 3		
3	8-Feb	Transistor Models	Ch. 3		
	10-Feb	Transistor Model and Process Variation	Ch. 3	Assignment 1 due on 2/14	
4	15-Feb	Wire Models	Ch. 4		
	17-Feb	CMOS Inverter 1	Ch. 5	Assignment 2 due on 2/21	
5	22-Feb	Review	Ch. 1-4		
	24-Feb	Mid-term 1	Ch. 1-4		
6	1-Mar	CMOS Inverter 2	Ch. 5		
	3-Mar	CMOS Inverter 3	Ch. 5		
7	8-Mar	CMOS Inverter 4	Ch. 5		
	10-Mar	Combinational Logic 1	Ch. 6	Assignment 3 due on 3/14	
8	15-Mar	Combinational Logic 2	Ch. 6		
	17-Mar	Combinational Logic 3	Ch. 6		
9	22-Mar	Combinational Logic 4	Ch. 6		
	24-Mar	Arithmetic Building Blocks 1	Ch. 11	Assignment 4 due on 3/28	Project Starts
10	29-Mar	Spring Recess			
	31-Mar	Spring Recess			
11	5-Apr	Review	Ch. 5-6		
	7-Apr	Mid-term 2	Ch. 5-6		
12	12-Apr	Arithmetic Building Blocks 2	Ch. 12		
	14-Apr	Arithmetic Building Blocks 3	Ch. 12		
13	19-Apr	Arithmetic Building Blocks 4	Ch. 12		
	21-Apr	Sequential Logic 1	Ch. 7		Project Report 1 due on 4/25

	26-Apr	Sequential Logic 2	Ch. 7		
14	28-Apr	Interconnect Issues	Ch. 9	Assignment 5 due on 5/2	
	3-May	Timing Issues	Ch.10		
15	5-May	Memory	Ch. 12		
	10-May	Memory	Ch. 12		
16	12-May	Future Outlook of Technologies			Final Project Report due on 5/16
17	17-May	Review	Ch. 1-7, 9, 10, 12		
	Friday, May 21	Final Exam: Friday, May 21: 1215-1430	Ch. 1-7, 9, 10, 12		