

San José State University
College of Engineering/Computer Engineering Department
CMPE 240 – Advanced Computer Design

Instructor:	Dr. Ahmet Bindal
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Office Hours:	Monday 1:30 – 3:00 PM
Class Days/Time:	Wednesday 3:00 – 5:45 PM
Lab Days/Time:	NA
Classroom:	Clark 226
Prerequisites:	CMPE 127 (with grade of "C" or better) Students who do not provide documentation of having satisfied the class prerequisite requirements <u>by the second class meeting will be dropped from the class.</u>

Course Web Page and Messaging

Copies of the course materials such as the syllabus, major assignment handouts, etc. may be found at: <http://www.engr.sjsu.edu/abindal>

You are responsible for regularly checking with the messaging system through MySJSU and the webpage at the link above.

Course Catalog Description

Architecture of a computing system including system bus, memory subsystems and peripherals. Unidirectional and bidirectional bus architectures; SRAM, SDRAM and FLASH memories and their interfaces with the system bus. Design of DMA, interrupt controller, transmitter/receiver, timers, display adapter, A/D and D/A converters and other system peripherals and their bus interfaces.

Program Outcomes

1. Being able to demonstrate an understanding of advanced knowledge of the practice of computer engineering, from vision to analysis, design, validation and deployment.
2. Being able to tackle complex engineering problems and tasks, using contemporary engineering methodologies and tools.

Course Goals and Student Learning Objectives

Course goals

CMPE 240 is an advanced logic design and architecture course that teaches various system buses, organization of different system memories and peripherals, and most importantly, their interface design with system bus using timing diagrams.

Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of forty-five hours over the length of the course (normally 3 hours per unit per week with 1 of the hours used for lecture) for instruction or preparation/studying or course related activities including but not limited to internships, labs, clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus.

Student Learning Objectives

1. Being able design a system bus
2. Being able to understand memory sub-systems and design their interface with a system bus
3. Being able to design system peripherals and interface them to the system bus
4. Being able to understand the overall system functionality

Required Texts/Readings

Required textbook

Ahmet Bindal, "Fundamentals of Computer Design: A Micro-Architectural Analysis and Design Study", ISBN 13: 978-938232-00-8.

Other Material (available from the class web site):

<http://www.engr.sjsu.edu/abindal/cmpe240.htm>

Classroom Protocol

You are expected to arrive in time for class. No cell phones and no open laptops are allowed in the lecture. Please be considerate of your fellow students.

Assignments and Grading Policy

Student Assessment

Midterm	30%
Term assignment(s)	30%
Final Examination	40%

0 to 49	F
50 to 59	D
60 to 69	C
70 to 79	B
80 to 84	B+
85 to 89	A-
90 to 100	A

- **No late assignments will be accepted.** An extension will be granted only if a student has serious and compelling reasons that can be proven by an independent authority (e.g. doctor's note if the student has been sick).

Descriptions of Assignments/Exams

Exams

Exams will be conducted closed book, comprehensive and will be based on the course material.

Once decided in the class, all exam dates are final. Students may retake a missed exam because of a health emergency or sickness accompanied by an official and signed doctor's report. Each case will be individually verified by calling the doctor's office. The retake exams may have more difficult set of questions than the ones asked in the original exam.

Term assignments

Term assignments require students to design and demonstrate part of a computing system and verify its functionality using hardware design tools. The projects are completed by a group of two students, and they should emphasize the product of a team work.

Students have the choice to design part of a computing system (or the entire system) that may consist of a bus, system memories, peripherals and bus masters interfacing a system bus using the hardware design language, Verilog.

Students may be asked to demonstrate the entire functionality of the system to the instructor in the form of an oral presentation where the instructor may ask technical questions and grade the team accordingly. The project requires an IEEE-compliant technical report.

The organization of the report will contain the following four sections:

1. Abstract and introduction

2. Description of the project which includes the architecture/block diagrams, functionality, timing diagrams, circuit schematics and components
3. Description of the overall learning experience and the difficulties encountered during implementation
4. Conclusions

Policy on Respect and Insubordination

Students who disturb the peace and harmony in class, behave disrespectfully to the instructor or his/her fellow students will be immediately dismissed from the class and reported to student affairs for disciplinary action.

Policy on Cheating

A student or students involved in a cheating incident in a test, homework, report, or lab project will receive an F in the course and will be reported to the judicial affairs office and subjected to disciplinary action.

I will personally notify you of any such findings or actions. All such reports will also be brought to the attention of the Chair of the Computer Engineering department. You have certain rights of appeal, which may serve to exonerate you.

Dropping and Adding

Students who do not provide documentation of having satisfied the class prerequisite and co-requisite requirements (if any) by the second class meeting will be dropped from the class.

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's Catalog Policies section at <http://info.sjsu.edu/static/catalog/policies.html>. Add/drop deadlines can be found on the current academic calendar web page located at http://www.sjsu.edu/academic_programs/calendars/academic_calendar/. The Late Drop Policy is available at <http://www.sjsu.edu/aars/policies/latedrops/policy/>. Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the Advising Hub at <http://www.sjsu.edu/advising/>.

University Policies

Academic integrity

Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The [University's Academic Integrity policy](#), located at

<http://www.sjsu.edu/senate/S07-2.htm>, requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The [Student Conduct and Ethical Development website](#) is available at <http://www.sjsu.edu/studentconduct/>.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy S07-2 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

Department Policies

- Students who do not provide documentation of having satisfied the class prerequisite or co-requisite requirements (if any) by the second class meeting will be dropped from the class.
- All non-proctored report (or similarly sized) assignments in courses where some of the final grade depends on prose writing will be submitted to Turnitin.com.

Engineering Student Success Center

The Engineering Student Success Center (ESSC) will help you move successfully from freshman to senior year, supporting and enhancing your learning and overall academic experience. ESSC is an inclusive environment that fosters collaboration, builds community and supports your smooth transition into college. It is located in Room 344 in the Engineering Building. The ESSC web site is located at <http://www.engr.sjsu.edu/students/essc>.

CMPE 240 Course Schedule

The schedule is tentative and subject to change.

Week	Topics
0	Introduction: explanation of the green sheet
1	Review of the digital design concepts: flip-flops, latches, registers, counters and timing diagrams
2	Continue to review digital design concepts: data-path and control circuits
3	Description and design of a unidirectional system bus and I/O
4	Description and design of a bidirectional system bus and I/O
5	System memories: SRAM and SRAM bus interface
6	System memories: SDRAM and SDRAM bus interface
7	System memories: E2PROM and FLASH
8	Midterm
9	DMA controller design and interface
10	Interrupt controller design and interface
11	Transmitter/receiver design and interface
12	Timer designs and interface
13	Display adapter design and interface
14	A/D and D/A converters
15	Continue to A/D and D/A converters and/or field programmable gate array architecture (if time allows)
16	FINAL EXAM (comprehensive)